HIGH-SPEED DRAMS, P. 34

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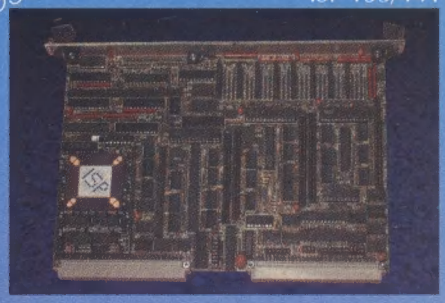

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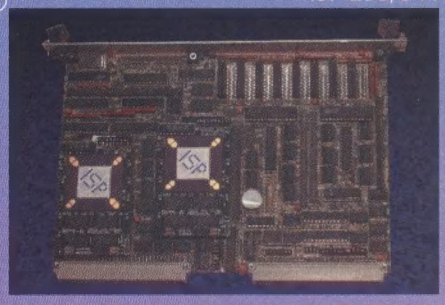

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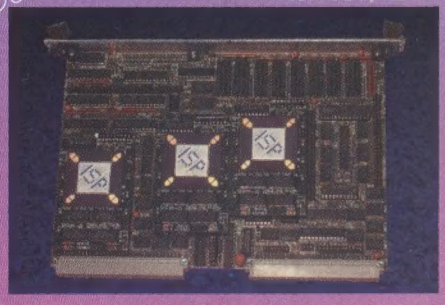

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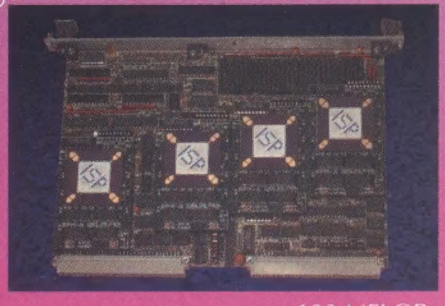

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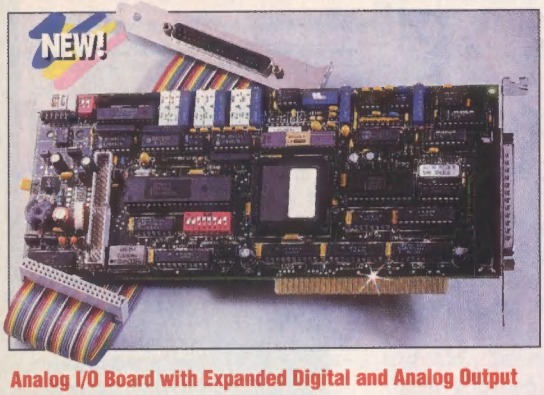

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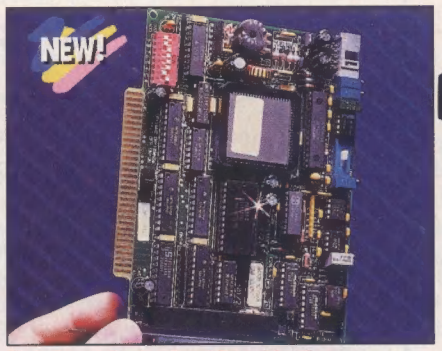

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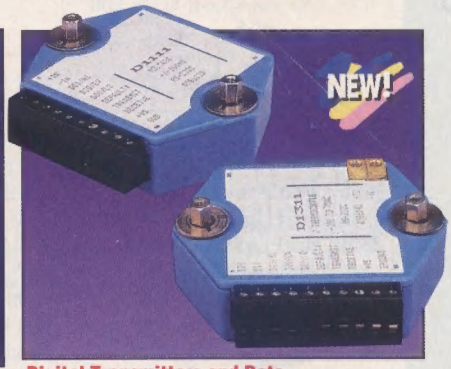

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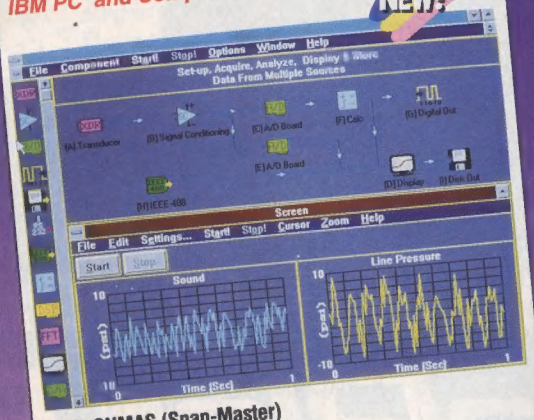

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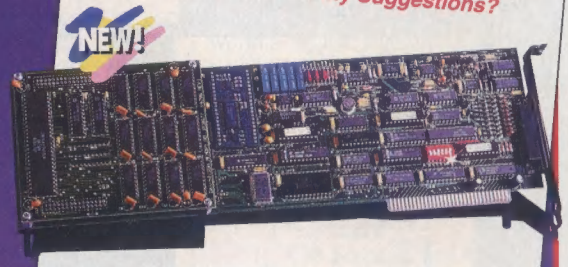

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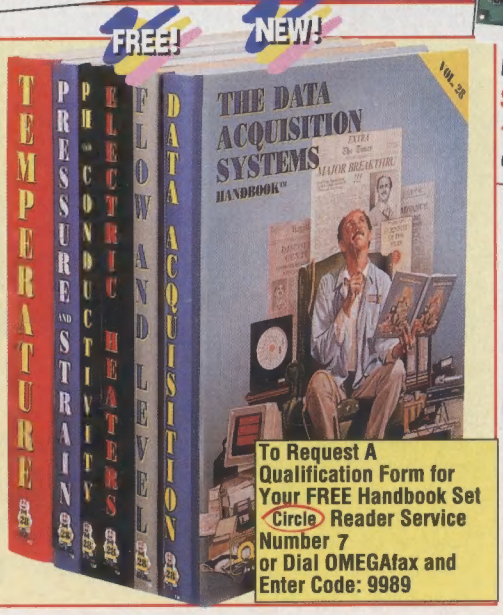

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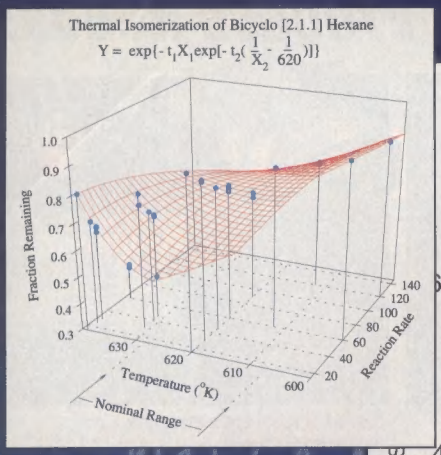

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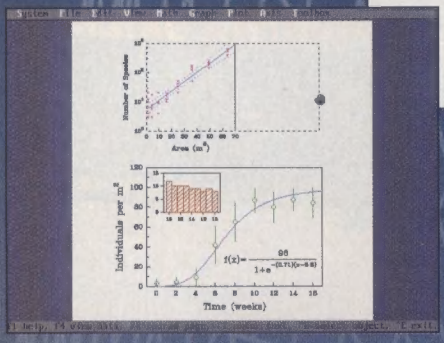

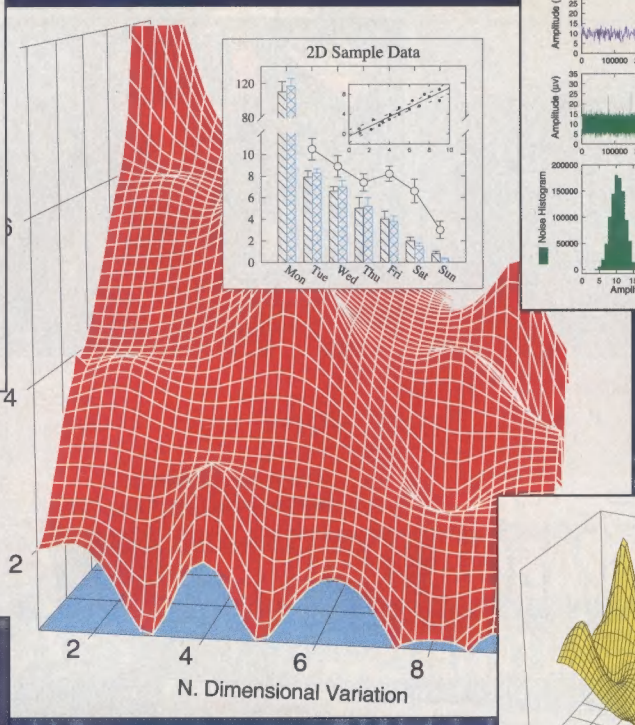

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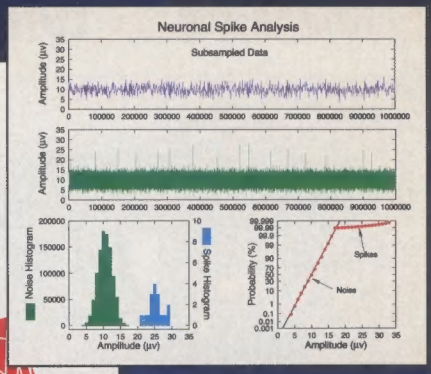
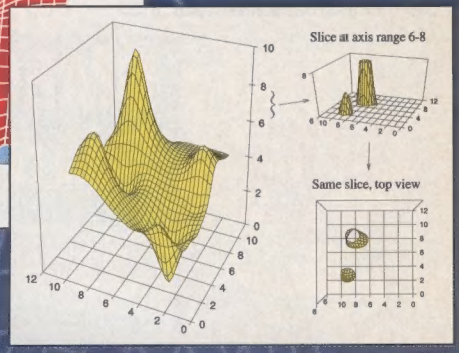


Graph huge datasets! This example contains over a million data points. Note data point sampling in top graph.



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Newslog

AUG 18. **IBM Corp.** said it will set up a joint venture with **Sears, Roebuck & Co.,** Chicago, through which the companies will merge their voice-and-data networking businesses to manage computer networks, both for Sears and for other corporate customers. Called Advantis, the company will operate one of the biggest private data networks in the world.

AUG 19. **ABB Asea Brown Boveri Ltd.** in Zurich, the Swedish-Swiss engineering group, said it had won a US $100 million deal to design and build the first big power generating plant in Puerto Rico in 20 years. The 248-MW gas turbine Cambalache station will be built near Arrecibo for the Puerto Rico Electric Power Authority.

AUG 19. **Wang Laboratories Inc.,** Lowell, Mass., said it had filed for court protection under Chapter 11 of the U.S. Bankruptcy Code and would cut 5000 jobs—or 38 percent of its workforce—in coming months. The company said it would now focus on big service businesses and the development and sale of software, and would shrink manufacturing operations.

AUG 21. **Honeywell Inc.,** Minneapolis, Minn., said it would receive $124 million from seven camera makers as part of a settlement involving rights to its autofocus technology. The agreements were negotiated separately with Canon, Eastman Kodak, Konica, Kyocera, Matsushita, Nikon, and Premier Camera Taiwan.

AUG 24. **Motorola Inc.,** Schaumburg, Ill., and **Amtech Corp.,** Dallas, announced they had set up a joint venture to develop a wireless electronic toll-collection system that would allow motorists to pay for tolls with a credit card or debit account. The system will use a standard radio frequency identification system for tollbooths throughout the United States.

AUG 27. **Philips Electronics NV,** the Netherlands, said it is selling the bulk of its test and measuring equipment business to **John Fluke Manufacturing Co.,** based in Everett, Wash. With the deal, Fluke, a manufacturer of test and measurement equipment, will return to the European theater after a five-year absence with a full sales, production, and service operation.

AUG 27. **Digital Equipment Corp.,** Maynard, Mass., and **Storage Technology Corp.,** Louisville, Colo., said they had formed a company to produce and sell thin-film heads for disk drives. The company, **Rocky Mountain Magnetics,** in Louisville, Colo., will concentrate first on inductive thin-film heads for original-equipment manufacturers and Digital's disk drives.

AUG 28. Japan's **NEC Corp.** said it and **AT&T Co.** had jointly developed technology to mass-produce next-generation computer memory chips. The company said the development will pave the way for production of 64M-bit memory chips on a commercial basis in 1995—and could be applied to 256M-bit chips.

AUG 29. Researcher **Kyoji Tachikawa** of **Tokai University,** Tokyo, said he had developed a way of halving the costs of fabricating the 10-μm-thick niobium-titanium superconducting wire that is to be used in the magnets of the Superconducting Super Collider. His method: block any damaging reaction between the fragile superconducting wire and its supportive copper sheath by adding silicon to the copper.

AUG 31. The **United States** announced it had agreed in principle to buy billions of dollars' worth of bomb-grade uranium from scrapped Soviet nuclear arms in an attempt to bolster the Russian economy and reduce risks of nuclear accidents or theft. The pact—the first such agreement—calls for at least 80 metric tons of highly enriched uranium to be diluted by the United States for sale as commercial reactor fuel.

SEP 1. **Sun Microsystems Inc.,** Mountain View, Calif., said it had signed a contract with a team of Russian computer experts to help the company develop advanced software for use with its workstations. The pact follows a similar joint research project that Sun announced in February, which led to the establishment of the Moscow Center of Sparc Technology.

SEP 1. **Lockheed Missiles and Space Co.,** Sunnyvale, Calif., said it had won two seven-year contracts worth $267 million from the **National Aeronautics and Space Administration** to maintain and service the Hubble telescope. Lockheed, a principal contractor in building the space telescope, said the contracts would employ about 150 workers at the Goddard Space Flight Center, Greenbelt, Md.

SEP 2. **IBM Corp.** said it would spin off its PC operations as a separate business, the IBM Personal Computer Co. The new unit, to be based in Somers, N.Y., starts life as the world's largest PC concern with inherited annual sales of about $7 billion. IBM has already formed PC subsidiaries in Europe and Canada.

SEP 2. The **National Aeronautics and Space Administration** said it would buy a Y-MP C-90 supercomputer from **Cray Research Inc.,** Eagan, Minn., to support its Ames Research Center's numerical aerodynamic simulation network. Cray was picked after a bidding battle with **NEC Corp.,** Tokyo.

SEP 3. **Toshiba Corp.** and **Asahi Chemical Industry Co.,** both in Tokyo, said they would form a joint venture to develop and manufacture lithium ion batteries that have twice the power of nickel cadmium batteries—currently the most popular kind of rechargeable battery. Mass production is to begin in October 1993 and will yield 500 000 batteries a month.

SEP 7. **China Great Wall Industry Corp.,** Beijing, said it had signed a contract to launch satellites for Intelsat, the world's biggest buyer of international telecommunications satellites. Go-ahead for the contract depends on an extension of a pact between the United States and China over the prices and frequency of Chinese launches.

SEP 10. The **Iranian** and **Chinese governments** announced that China will provide Iran with its first 300-MW nuclear power plant. China is currently building a small nuclear research reactor for Iran in Isfahan.

SEP 11. **Fujitsu Ltd.,** Tokyo, said it had developed a supercomputer, the VPP500, capable of handling a maximum of 355 billion floating-point operations per second (gigaflops). The company said it had found a way to make large numbers of small supercomputers, each capable of 1.6 gigaflops, work together to yield a network through which data can be run at 800 Mbytes a second.

Preview:
OCT 26–28. "Electronic Messaging '92," the **Electronic Mail Association's Annual Conference,** is to be held in San Francisco. Topics will include Internet, wireless communications, and Pacific Rim messaging perspectives [see related special report, "Electronic Mail," pp. 22–33]. For information, call 703-875-8620.

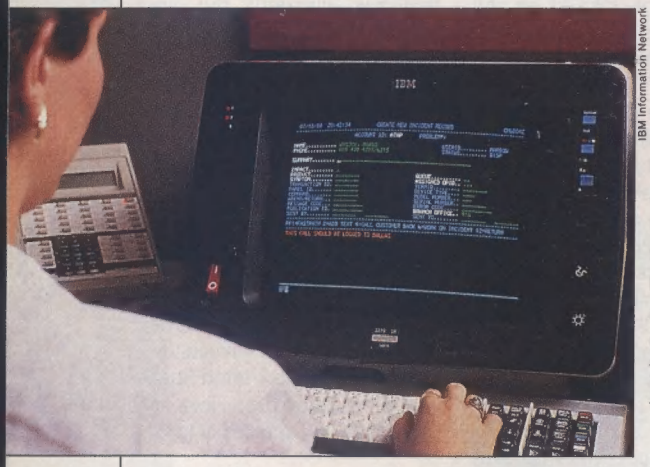
COORDINATOR: Sally Cahur

OCTOBER 1992 Volume 29 Number 10

IEEE SPECTRUM

SPECIAL REPORT

22 E-mail: pervasive and persuasive



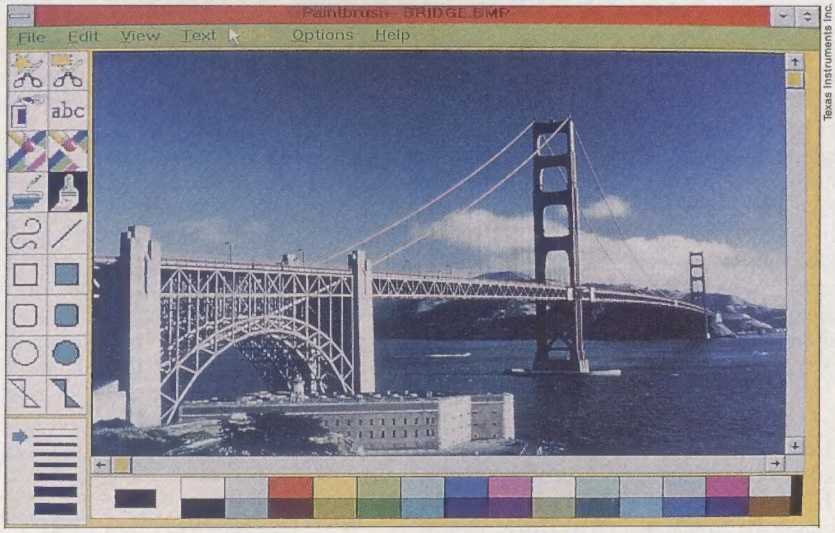
IBM Information Network

The global network has the power to break through boundaries of time, distance, and politics, *Tekla S. Perry and John A. Adam* **22.** Engineers using e-mail collaborate on complex designs with colleagues they've never met, *Tekla S. Perry* **24.** Fantasy games, personalized magazines, and even digital dating draw leisure-time users into the net, *John A. Adam* **29.** E-mail networks are empowering democratic actions in governments of all sizes from small U.S. towns to the former Soviet Union, *Tekla S. Perry* **30.**

SPECIAL REPORT

34 High-speed DRAMs

A group of industry experts reports that main-memory chips at last are catching up with microprocessors—in various ways, *Richard Comerford and George F. Watson* **34.** Fast computer memory, *Ray Ng* **36.** Fast DRAMs for sharper TV (see below), *Roelof H.W. Salters* **40.** A new era of fast dynamic RAMs, *Fred Jones, Betty Prince, Roger Norwood, Joe Hartigan, Wilbur C. Vogley, Charles A. Hart, and David Bondurant* **43.** A fast path to one memory, *Mike Farmwald and David Mooring* **50.** A RAM link for high speed, *Stein Gjessing, David B. Gustavson, David V. James, Glen Stone, and Hans Wiggers* **52.** Fast interfaces for DRAMs, *Richard C. Foss, Betty Prince, Richard Rodgers, David B. Gustavson, David V. James, Glen Stone, and Stephen Kempainen* **54.**



Texas Instruments Inc.

ADVANCED TECHNOLOGY

58 Fuzzy fundamentals

By EARL COX

Applied where appropriate, fuzzy logic can greatly simplify many systems. But successful implementations require that the designer thoroughly understand the system dynamics. And it's a good idea to follow an orderly design procedure.

POWER

62 Consolidating European Power

By HENRI PERSOZ and JEAN REMONDEULAZ

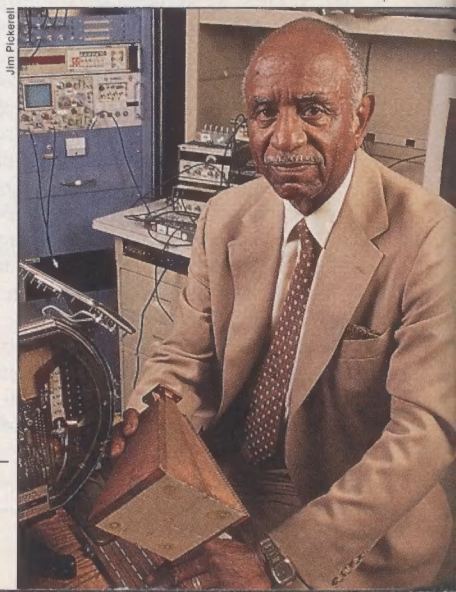
Energy interdependence between west and east Europe is expected to grow as plans go into effect to increase the electric energy interchange between the two regions. Synchronization of the grids is a preferred option.

PROFILE

70 Howard S. Jones Jr.

By JOHN A. ADAM

Over a 37-year career, Howard S. Jones Jr.'s work on antenna design did much to make U.S. Army missile technology possible. Now in semi-retirement, Jones does his utmost to encourage minority students to study engineering.



Jim Pickerell

SYSTEMS

66 The art of architecting complex projects

By EBERHARDT RECHTIN

Jet Propulsion Laboratory

How a system is created, designed, and built blends art and engineering. NASA's Deep Space Network is the product of such a process. Here, great antennas peer into space from its Canberra, Australia, station. The article describes the architecting process and provides additional examples.

SPECTRAL LINES

21 Challenges to management

By DONALD CHRISTIANSEN

"Scientific management" gives ambiguous guidance today. Nevertheless, managers have to select among traditional, perhaps outmoded, concepts and contemporary techniques, perhaps fads, to develop a self-consistent management process.

Cover: Electronic messages travel over a global network unbounded by time zones, distance, or political entities in Gus Sauter's conceptual illustration. With e-mail, an engineer can communicate with a colleague halfway around the world as easily as with a co-worker down the hall. The technology, still in its infancy, is changing society as well as business. *Spectrum*'s Special Report on e-mail begins on p. 22.

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Alpha is not omega

As PA7100 product manager for Hewlett-Packard Co.'s system technology division, I wish to comment on "How DEC developed Alpha" by Richard Comerford [July, pp. 26–31]. The author compared DEC's 150-MHz Alpha prototype, at 110 SPECmarks, to HP's Series 730 workstation at 77 SPECmarks. This is an apples-to-oranges comparison.

A better comparison would be to HP's PA7100 chip, which was announced at the same time as Alpha. The PA7100, at 100 MHz, will produce over 130 SPECmarks.

An exact comparison will have to wait until both companies announce systems, but as the article notes, "to achieve superiority, [Alpha] will have to be at least 50 percent faster than its competitors when it comes to the market." Clearly, Alpha has failed to achieve this goal.

Linley Gwennap
Cupertino, Calif.

Mixed signals

In "Grounds for signal referencing" by Anthony N. St. John [June, pp. 42–44], the author appears to have overlooked a few of the basics. Although he refers to the National Electrical Code (NEC), he does not use its terminology. For example, what he calls the "neutral" is in the NEC called the "grounded conductor." A neutral conductor is defined in the NEC's Note 10 to Tables 310-16 through 310-31 as a conductor that "carries only the unbalanced [sic] from other conductors, as in the case of normally balanced circuits of three or more conductors." This does not apply to the wiring diagram of Fig. 1. And the yellow conductor could better be called an "isolated equipment grounding conductor." Finally, in even an isolated ground receptacle, the "wide" slot is connected to the grounded (white) conductor.

Vernon H. Waight
San Francisco

The author responds:

I agree completely that the National Electrical Code is the paramount reference for electrical safety requirements. Any possible confusion caused by the information presented in my article must yield to the absolute authority of the NEC. For example, the precise use of the term "grounded conductor" used in the NEC takes precedence over the term "neutral," which is also used in the NEC Handbook.

Figure 1 was intended to illustrate the more typical electrical installation, which most often does not use any insulated equipment grounding receptacles (as permitted in Section 250-74, Exception No. 4). The purpose was to illustrate a communications ground loop.

The comments on Fig. 2 (as well as more on Fig. 3) were noted in "Corrections" [July, p. 56]. As the figures appeared, they would obviously have been more appropriately captioned as "common wiring errors." The original artwork, to which I refer readers for correct information, was from FIPS PUB 94.

I take full responsibility, and apologize, for any confusion that may have been caused in the presentation of the article. I do hope, however, that the main point I wanted to make—never take a signal reference ground for granted—prevailed.

Get the fuzz out

The article "Fuzzy logic flowers in Japan" [July, pp. 32–35] reminds me of what happened when artificial intelligence was "discovered" a few years ago. At that time, I worked for Hydro-Quebec and, almost as a hobby, I had developed an expert system capable of analyzing the events taking place in our very complex and critical extrahigh-voltage network. The information contained in the network's data bank was very rich and complete, and the expert system was able to read the data bank, determine a difference between voluntary and involuntary events, and, after 30 seconds, print a very complete sequence, down to the millisecond, of what had happened.

I developed the system even though I did not know at the time that I was using inference motors, forward and backward chaining, and other related subtleties. These I discovered later when the scholars jumped onto the wagon and organized congresses, symposia, and fancy conferences using satellites—at which, after inventing a new dedicated jargon, they pontificated first about intelligence and then about expert systems, complicating practically everything that up until then had been logical and simple, without, finally, ever producing anything of practical value.

After reading about fuzzy logic, I am afraid history is repeating itself. Many years ago I headed a group of very experienced control engineers who, using a minicomputer, developed a control system for a hydroelectric generating plant. No fancy equations, no sophisticated models, no specially developed software. Everything—from starting the optimal number of units to synchronizing them to the network and managing the load—was automatic and had been programmed by plain engineers using the "good enough" approach. It worked beautifully.

At the time none of us knew about fuzzy logic, and even today I could do it again without reading a book about the matter. Right now, the Japanese are inundating the market with washing machines, cameras, car electronics, videos, etc., using this old common sense logic, which has been newly christened "fuzzy logic." If North American industry gets fooled again by scholars into thinking that this is a very academic and complex theory requiring a dedicated vocabulary and specialized studies, as with artificial intelligence, it is going to take a long time before we can compete with the Japanese in this area.

Sergio del Pozo
Westmount, Que., Canada

Someone is watching you

The article "Improving on police radar" by P. David Fisher [July, pp. 38–43] was interesting. Unfortunately, the system described is well behind the state of the art in European countries.

Specifically, the Germans have had a system in place for some years that not only photographs the car from the rear, but does so also from the front and side, and with sufficient resolution that the driver is easily identified. That virtually eliminates the problem of the owner claiming that he or she was not driving the car at the time of the infraction.

I learned about this system from a nephew who was caught by the system in Heilbronn. He was going to plead innocent until he was handed copies of the photographs. In his words, "There I was driving the car and there was Michael in the passenger seat. I couldn't deny it. I paid the fine and got out of there."

For other ways in which the Europeans are ahead of the United States in applications of technology, look at their unattended (and fee-collecting) parking garages and lots. Magnetic stripes on the parking tickets not only record time of entry and time of paying the fee, but also verify the fact that you have not exceeded the time allowance between fee payment and reaching the exit gate. You pay the fee by inserting the ticket into a machine located near any pedestrian entrance to the garage and in-

(Continued on p. 75)

Calendar

Meetings, Conferences and Conventions

OCTOBER

International Carnahan Conference on Security Technology (AES et al.); Oct. 14–16; Atlanta Penta Hotel, Atlanta, Ga.; Lawrence D. Sanson, 186 Woodwalk Court, Nicholasville, Ky. 40356; 606-223-9840.

International Symposium on Systems, Man and Cybernetics (SMC); Oct. 18–21; Knickerbocker Hotel, Chicago; Richard Saeks, Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, Ill. 60616; 312-567-3221.

VHDL International Users Forum (COMP); Oct. 18–21; Omni Shoreham Hotel, Washington, D.C.; VHDL International Inc., 407 Chester St., Menlo Park, Calif. 94025; 800-554-2550, 415-329-0578; fax, 415-324-3150.

Joint Power Generation Conference—JPGC '92 (PE); Oct. 18–22; Hyatt Regency Hotel, Atlanta, Ga.; Marisa Scalice, American Society of Mechanical Engineers, 345 E. 47th St., New York, N.Y. 10017; 212-705-7053.

Third International Conference on Solid-State and Integrated Circuits Technology (ED); Oct. 18–24; Century Hotel, Beijing, China; Zhou Mengqi, Chinese Institute of Electronics, Nongzhanguan Nanlu No. 12, Room 2310, Beijing 100026, China; (86+1) 500 1144, ext. 2310; fax, (86+1) 500 5233.

Fourth Symposium on the Frontiers of Massively Parallel Computation (C); Oct. 19–21; McLean Hilton Hotel, McLean, Va.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

Joint Dimacs/IEEE Workshop on Coding and Quantization (IT); Oct. 19–21; Dimacs Rutgers University, Piscataway, N.J.; Nader Moayeri, Department of Electronic and Computer Engineering, Rutgers University, Piscataway, N.J. 08855-0909; 908-932-5253; fax, 908-932-5313.

Sixth Annual Leesburg Workshop on Concurrent Engineering (R); Oct. 19–22; Xerox Training Center, Leesburg, Va.; Henry N. Hartt, Vitro Corp., Suite 300, West Wing, 600 Maryland Ave., S.W., Washington, D.C. 20024; 202-646-6339.

(Continued on p. 18)

IEEE members attend more than 5000 IEEE professional meetings, conferences, and conventions held throughout the world each year. For more information on any meeting in this guide, write or call the listed meeting contact. Information is also available from: Conference Services Department, IEEE Service Center, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855; 908-562-3878; submit conferences for listing to: Ramona Foster, *IEEE Spectrum*, 345 E. 47th St., New York, N.Y. 10017; 212-705-7305.

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Graphics

The genius is in the detail

In the beginning, there was the wire frame, the stick-figure world that was the genesis of three-dimensional computer graphics. Then came the Gouraud-shaded triangle, and the technology took on a whole new dimension (the *z* dimension, in fact).

Now, in a generational change, impressive realism is being standardized through the widespread adoption of two techniques: the smoothing (or anti-aliasing) of lines and the edges of figures on the screen; and the routine covering of surfaces with textures.

The problem is that the rush of technology advances is greatly complicating matters, said Douglas Voorhies of Silicon Graphics Inc., Mountain View, Calif., who also chaired a panel session on the future of graphics hardware last July 31 at the annual Siggraph conference in Chicago. "The same technologies and improvements that have pushed [ordinary microprocessors] like crazy have offered the opportunity for equivalent advancement in graphics; but it's much less clear what to do with them, because the field is so immature," he said. The design of bit-mapped computer graphics hardware may be said to have begun with the Xerox Alto, the first of which was built 19 years ago, he noted.

Graphics hardware designers are applying technology toward improving image quality, improving raw performance (such as rendering lower-quality images with great speed), and providing interactivity. As might be expected, different designers (and companies) are emphasizing different objectives and pursuing them in different ways.

Anti-aliasing and texture-mapping add realism to computer images, such as this still from a driving simulation on Silicon Graphics' new RealityEngine.

Computer graphics systems have a front end, known as a floating-point or geometry engine, which manipulates the myriad triangles and polygons that make up a computer image. The geometry engine performs all calculations necessary to orient and illuminate figures for a particular scene. There is also a back end: a drawing processor, or rasterizer, which transforms the figures from the geometry engine into pixels on the screen. Thus specialists often speak of a graphics pipeline, into which polygons flow by the many thousands per second, and out of which video emerges.

Rasterization is where the "real excitement is," in Voorhies' opinion. This is where texture mapping and anti-aliasing are done, the latter by fractional illumination of pixels. When pixels can be only bright or dark, diagonal lines or edges often look jagged, because the position of the pixels may not correspond well to the orientation of the line. But with the brightness of the pixel reflecting how much the line or edge encroaches on it, the diagonal looks smooth.

This technique is used in Silicon Graphics' RealityEngine, a top-of-the-line graphics system introduced in July. The machine's front end is based on an array of up to eight Intel i860 microprocessors, while rasterization is done by a back end based largely on custom ICs. According to Silicon Graphics, the RealityEngine can draw 600 000 anti-aliased, textured polygons per second. "It's the first machine able to fill the whole screen with anti-aliased, texture-mapped polygons at a real-time rate," said Voorhies.

A rather different approach to achieving high speed and high quality has been under development for 12 years at the University of North Carolina's computer science department. Commercial graphics systems, such as the RealityEngine, mix different forms of parallelism. In the front end, object parallelism reigns: different processors work on different objects, typically triangles, in the scene to be displayed. The back end, however, is pixel-parallel: multiple rasterization processors, each of which has its own piece of frame buffer memory, control subsets of the pixels on the screen.

In the UNC machine, called Pixel-Planes, object parallelism prevails from geometry processing all the way through rasterization. To display images on the screen, the machine uses a technique called screen subdivision, according to John Poulton, research associate professor at the Chapel Hill university. Each rasterization processor is associated with a portion of the screen; to the extent that different small primitives (triangles or polygons) fall into different screen regions, they can be processed in parallel on the multiple rasterizers. To produce the whole scene, the fragmentary images from different regions are concatenated into a standard frame buffer.

The catch is that if a figure falls into two regions at once, it is rendered twice. "We lose as much as 20 percent of our performance that way," Poulton said. "But it's no big deal."

The architecture is based on the idea of integrating on the same IC the rasterizer processors and the frame buffer memory; the idea was proposed in 1981 by Henry Fuchs (also of UNC) and Poulton. Integrating the rasterizers with the frame buffer memory permits high bandwidth between the two, which is critical to high performance.

The first two generations of Pixel-Planes were unveiled in 1986 and 1990, and a third incarnation, called PixelFlow, is now being built. PixelFlow is object-parallel using a different method, called image composition. With this method, each rasterizer is associated with a portion of the primitives, but paints a full-screen image. Images from multiple rasterizers are pieced together, based on visibility information, in a special hardware network to form the final image.

In a large configuration with 20 rasterizing boards, the second-generation machine, called Pixel-Planes 5, can sustain a rate of 2.3 million Phong-shaded triangles per second, Poulton said (the triangles in this case are not anti-aliased, but anti-aliasing is well within the machine's capabilities). All told, Poulton believes the machine is at least twice as fast as the fastest commercial systems.

Scheduled for completion by the end of 1993, PixelFlow will also rely on a series of processing boards. Each will be capable of one to two million textured, complex-shaded polygons per second, Poulton estimated, and the entire system should support at least 40 or 50 boards. Thus overall performance could approach 10 000 000 textured, shaded polygons per second, he said.

COORDINATOR: Glenn Zorpette

REQUIRED READING

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Donald Christiansen, *Editor and Publisher*

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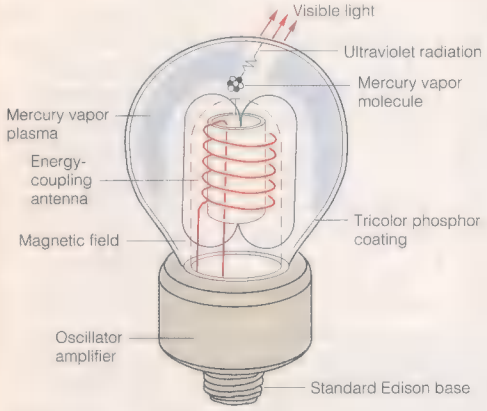
Innovations

Bright idea

An electronic light bulb with an expected life of 20 years combines the compactness and light intensity of incandescent bulbs with the energy efficiency of fluorescent lamps. Called the E-lamp (for electronic lamp), it was developed by Intersource Technologies Inc. and engineered by Diablo Research Corp., both based in Sunnyvale, Calif., and should enter beta-testing late this year. The companies expect to introduce it as a consumer product in the second quarter of next year.

The E-Lamp is best described as an RF-excited electrodeless fluorescent light source. A 13.56-MHz crystal-controlled oscillator generates RF signals that are amplified and then emitted into the glass bulb through an energy coupling antenna [see illustration]. The RF energy ionizes mercury vapor inside the glass assembly. (The ionized plasma becomes a conductive ring, essentially acting like the secondary of an air-coupled transformer, where the primary is the coupling antenna.) As the mercury ions transit between energy states, they resonate at the ultraviolet wavelength of 254 nm. The emitted ultraviolet radiation strikes the phosphor coating on the inside of the glass bulb, and the phosphors then emit the visible light.



Source: Intersource Technologies Inc.

According to Intersource director Thomas Moore, by using the appropriate mix of tricolor phosphors, the lamp can produce a color temperature ranging from 2700 K to 4000 K, or from red to blue, including a very close reproduction of standard incandescent lighting.

But it is much more efficient than incandescent bulbs, which lose 95 percent of their energy in heat. The E-lamp requires only 25 W of ac power to produce as much light as a 100-W incandescent bulb. Because the E-Lamp has no glowing filament to burn out, it will operate as long as the phosphors and the electronics are intact. The phosphors are expected to last about 20 000 hours before degrading to the point where the lamp has lost 30 percent of its intensity.

Actually, the idea for the E-Lamp is not new; work was begun in the 1970s by physicist Donald D. Hollister with some funding from the U.S. Department of Energy (then called the Energy Research and Development Administration).

But the earlier work was stalled by certain practical difficulties—primarily the production of significant RF interference. Now, with a proprietary technique for eliminating the RF interference (which Moore declined to explain until the patent application is completed), those difficulties have been removed.

The first commercial application for the E-Lamp is expected to be in reflector lighting for indoor flood lights. The price is likely to be comparable to that of existing compact fluorescents.

Packing density

Data densities approaching 7 gigabits per square centimeter may be reached on conventional magneto-optic materials using a revolutionary new data-storage technique. Demonstrated by a team of researchers at AT&T Bell Laboratories in Murray Hill, N.J., it achieves nearly 100 times the density of today's best commercial magneto-optic methods and 300 times that of current magnetic storage capabilities.

According to the team's leader, Eric Betzig, a member of the technical staff in the semiconductor physics research department, the secret of the technique is to write and read the bits by shining laser light through a tapered optical fiber instead of through a lens.

Conventional magneto-optical data-storage systems write a bit by focusing light from a semiconductor laser through a lens to heat a spot on the magneto-optic material. Heating gives the spot a magnetic orientation different from its surroundings. The bit can be read using a laser of lower power than the one that wrote it.

The smallest bit that can be written by such a lens-based system is limited by the diffraction of light to about the wavelength of the light shone through the lens: approximately a micrometer in diameter for an infrared laser, or half a micrometer for a blue laser. The lensless technique can write

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Books

Nirvana is in the NAND gates

Barrett Hazeltine

The American Replacement of Nature: The Everyday Acts and Outrageous Evolution of Economic Life. *Thompson, William Irwin, Doubleday, New York, 1991, 159 pp., $20.*

Pop quiz: what do Walt Disney's Epcot Center, Cable News Network, artificial intelligence, and processed food have in common?

Answer: all manifest a drive in the United States to replace education with entertainment, history with an electronic collage of sound bites, mind and soul with NAND gates, and in general, nature with technology. At least, this is the thesis of the author, a resident scholar at the Cathedral of St. John the Divine in New York City, who has taught at respected universities in North America. From the book it is clear that he has diverse knowledge and insights, and his writing varies from provocative to outrageous. This is hardly your typical engineering text.

Three main chapters are built around Disney, CNN, and artificial intelligence. Disney's genius was in making every visitor a star in his or her own movie—a replacement of nature. In Disneyland, evil, in the form of elaborate mechanical monsters, is kept at a safe distance. Meanwhile, visitors are empowered by technology, in the form of the carts that whisk them safely by the monsters.

"Disneyism" is part of an electronic (communication-rich) society, a post-literary culture that appeals to everyone. It is a religion of happiness without a guru, an evangelist, or a sword—one in which entertainment has replaced education.

According to Thompson, the electronic capabilities and common aspirations that have globalized culture are doing the same thing to economies. This transformation of culture and globalization of both culture and trade are irreversible, he argues. But in a century or two they will lead to a new structure of consciousness, just as after the Middle Ages a religion-centered world view largely gave way in the end to scientific rationalism.

CNN made the Persian Gulf war "a form of [global] informational integration," he asserts. Global electronics have the power to continue linking individuals, thus restraining any dictator. Television, though, trivializes history even as it replaces it. The casual viewer cannot tell what is news and what is an advertisement for an upcoming "docudrama." The pace and the information processing work against careful reflection, so principles become mere signs, reducing civilizations to collectives and making moral judgments meaningless.

The ultimate replacement of nature would be the transference of a person's mind from the brain into a computer, giving rise to a form of immortality. Thompson is repelled by this variety of reincarnation and argues that it is in any case impossible, because genetic structure is too complex to be captured in a finite-state machine. Engineers are contrasted here with poets: the former want to leave nature; the latter, to love it.

A dominant theme is what Thompson calls a religious commitment in the United States to technology that allows "escape from the imperfect condition of a false nature," and avoidance of "the embarrassment of sex and the insult of death." The economic life of the book's subtitle shows up in the text as descriptions of the world economic order: "the U.S. pulled out of the depression by a clever maneuver that shifted the source of economic value from the past to the future." Concern is also expressed about our society's emphasis on consumption; people want to buy substitutes for nature.

Much of the book's excitement and value come from its provocative side remarks. For instance, to Thompson, the insipid music permeating public spaces dissolves individuality, because one cannot escape it or its influences. What makes science different from art is that art (a painting by Picasso, for example) cannot be repeated. Also, Hollywood and Disneyland spatialize time—in one place, a viewer or visitor can see Benjamin Franklin; in some other place, World War I aviators, and so on. The sense is lost that history moves linearly from week to week, decade to decade, and century to century.

Parts of the book may be offensive to engineers. The creativity and aesthetic value of the various technologies described are not often recognized. Nor is much guidance offered for the engineer working in the laboratory or on a terminal who wants to behave responsibly. Thompson is worried about the replacement of nature but does not show convincingly why people should be kept away from Epcot or CNN—or why engineers should not work on virtual reality.

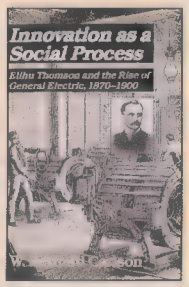
Nonetheless, the reader does not have to agree with or even understand all of this book to learn from it or enjoy it. The issues covered are of great importance. I found much food for thought and, ironically, more than a little entertainment as well.

Barrett Hazeltine is professor of engineering and associate dean of the college at Brown University in Providence, R.I. During the 1991–92 academic year, he held the Robert Foster Cherry chair for distinguished teaching at Baylor University in Waco, Texas. He has been active in the New Liberal Arts Program of the Alfred P. Sloan Foundation, which is concerned with the teaching of technology to students outside engineering.

He brought good things to life

George Wise

Innovation as a Social Process: Elihu Thomson and the Rise of GE, 1870–1900. *Carlson, W. Bernard, Cambridge University Press, Cambridge, England, and New York, 1991, 377 pp., $44.50.*



Elihu Thomson (1853–1937) would be worth remembering for his unusual constellation of personal qualities and technical skills, even if he had not been one of the most prolific U.S. inventors and the joint forefather, with Thomas Edison, of General Electric Co. His 696 patents make him the third most productive inventor ever; yet he concentrated exclusively on invention for fewer than 25 of his 84 years.

He vigorously marketed his inventions, yet held up their introduction in order to ensure safety by testing them in his own house (and was so careful of GE's money that he used only "factory second" light bulbs). He was stubborn enough to block the sale of a company because his patents had not been exercised with due diligence, yet cooperative enough to work harmoniously with manufacturers and marketers, in a manner that many people today think happens only in Japan.

That last quality, teamwork, is Carlson's focus in this illuminating new biography. His purpose is not so much to tell Thomson's life story as to use Thomson to explore in detail how an individual becomes an innovator. Carlson finds that in Thomson's case the keys were teamwork, craftsmanship, and integrity.

Chronologically, craftsmanship came first. Throughout his life, Thomson elegantly

(Continued on p. 16)

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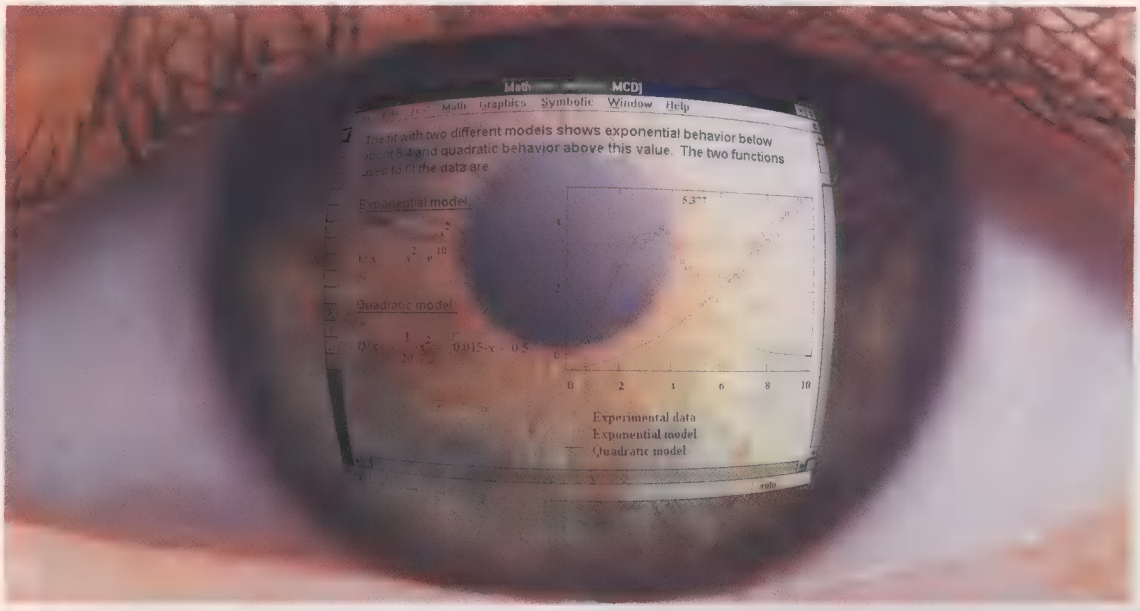

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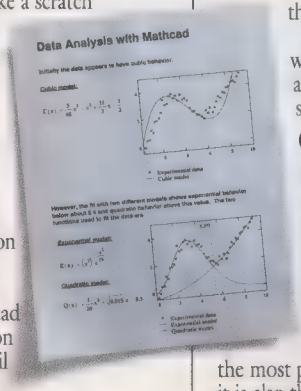

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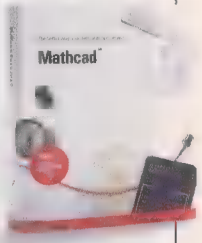

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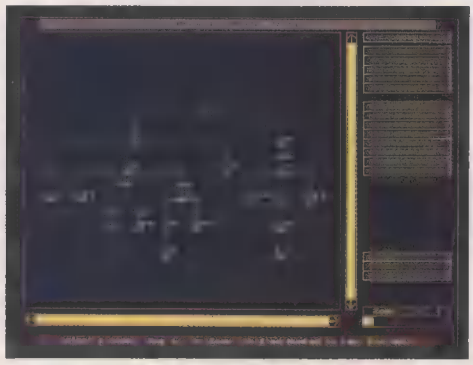
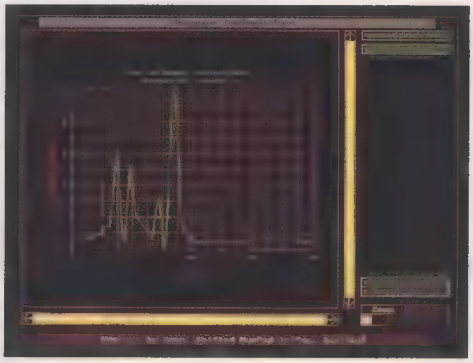


EDSA Transient Stability program has been designed to study the transient stability of electric power systems by means of time-domain simulation. The program is capable of simulating the dynamic behavior of a power system due to one, or a series of faults/disturbances within the system. Symmetric three-phase faults/disturbances and non-symmetric faults/disturbances can be simulated. Stability improvement measures, such as automatic recloser of a line, generator tripping, and load shedding can also be included.

Harmonics Analysis



This graphically simulated program allows the user to measure Harmonics and input the result as the time-domain into the EDSA Harmonics library. User can edit, add and modify source and filter libraries. User can also open windows at a specific bus and view frequency scan or Total Harmonics Distortion.

* all EDSA programs are fully verified and validated. IEEE, AEP, ANSI, long hand calculations and third-party test files are included.

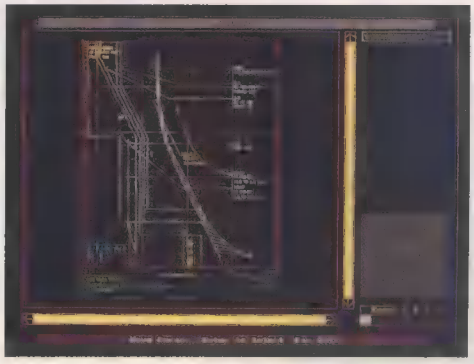
* EDSA programs are unique in their ability to handle HYBRID, Three-Phase, Single-Phase, Balanced, Unbalanced, AC and DC systems.

* Complete interface with AutoCAD and Microstation with back annotation.

* Over 20,000 devices built in.

* Pre-packaged industry standard symbols on a convenient pull-down menu.

Protective Device Coordination



A network intelligent program which communicates with feeder and BUS data files and allows the user to place protective devices all over the network (not just in an ascending line). The program chooses fault values from the Short Circuit program. Creates plot curves on log-log paper with no voltage limitations.

Motor Starting

EDSA Motor Parameter Estimation, Motor Performance, Motor Torque Simulation (SCKVA/Slip Method), and Motor Re-Acceleration include complete library of starting devices. EDSA Transient Time-Domain Motor Starting allows the user to start motors in time intervals.

SOME OF THE PROGRAMS CURRENTLY AVAILABLE

*** Harmonics Analysis * Transient Stability * Active Optimal Power Flow * Fault Analysis - Single-/Three-Phase/AC/DC/ Balanced/Unbalanced/Loop/Radial/Multi Utility/ANSI/IEEE/IEC * Fast Decoupled - Newton Raphson/AC/DC/Single-/Three-Phase/Balanced/Unbalanced/Multi Swing Bus/Constant I/Z/KVA Load Flows * Electromagnetic Transient Analysis * Motor Starting Voltage Dip Load Flow - Impedance Division Method * Wire Sizing - NEC/Bare/IEC/Neher-McGrath * Power Factor Correction * Electrical Schedules * Positive & Zero Sequence * Protective Device Coordination * Transformer Sizing * Generator Sizing * Battery Sizing * Cable Pulling * Ground Grid Design * Capacitor & Capacitor/Reactor Start of Large Motors * Shielding Effectiveness.**

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Books

(Continued from p. 12)

made his own tools, whether telescopes and microscopes or camping gear and small arms ammunition. Teamwork came next. Thomson's capability and class attracted partners. The first, physicist Edwin Houston, helped launch Thomson's career in science; Thomson kept Houston's name on his companies long after the partnership had dissolved.

Another partner, ▪ Philadelphia arc light sales agent, hired Thomson and persuaded him to become a full-time inventor. He soon helped Thomson hook up with a New Britain, Conn., capitalist—but, unfortunately, one whose combination of speculative proclivities and weak nerves ended in his suicide.

This led, in 1882, to the crisis of Thomson's life: finding a new business partner, so he would not have to go it alone. ''The tension of having to make business arrangements during the summer of 1882,'' Carlson notes, ''made him physically ill.'' The cure came in the form of a one-time shoe merchant, Charles Coffin. Carlson traces how ▪ successful company, Thomson Houston, emerged at the forefront of 1880s' electrical technology through ▪ combination of teamwork and tension among a triumvirate of Coffin, leading finance and marketing; Thomson, leading development and design; and Edwin Rice, Thomson's former student (and a future president of GE), leading manufacturing.

Coffin, like Andrew Carnegie, concluded that pioneering did not pay, but that following close on the heels of pioneers did indeed. There were four major technologies in the early electrical era: arc lighting, incandescent lighting, street railways, and alternating current. Thomson-Houston pioneered none of them. Yet it ended up swallowing or dwarfing all the companies that did.

Coffin was also a pioneer of sorts in junk-bond marketing and in mergers and acquisitions. Carlson's account of Coffin's ultimate merger, the creation of GE, draws on sources (such as the Higginson and Morgan papers) not used by previous accounts and concludes, contrary to some of those accounts (though quite sensibly), that the main reason for the merger was to limit competition.

Thomson needed Coffin. But did Coffin need Thomson? Could Coffin have hooked on to any competent inventor, instructed him to copy or improve on the state of the art, and ended up with ▪ winning company? Carlson says no. Technologists who could do the reverse-engineering job needed were not all that common in 1882. And Thomson did more than mere reverse engineering. He added elegant improvements to the work of Charles F. Brush in arc lighting and to the alternating-current system pioneered by William Stanley and George Westinghouse.

In developing that ac system, Thomson outshone Coffin in one important area: integrity. In December 1889 Coffin asked Thomson to write a popular article assuring the public of the safety of alternating current. Thomson refused to do so, summing up his reasons in a letter penned on Christmas Eve: ''I have no panacea,'' he wrote. ''No improvement of our modern civilization has ever been introduced but that involved considerable risk.'' While other electrical inventors waged a noisy and mean-spirited debate about the merits of ac versus dc, Thomson applied craftmanship, integrity, and teamwork toward reducing that public risk. The safety features that resulted, such as the grounded secondary, are his finest legacy.

George Wise is a communications specialist at the GE Research and Development Center in Schenectady, N.Y. He is the author of Willis R. Whitney, General Electric, and the Origins of American Industrial Research *(Columbia University Press, New York, 1985).*

COORDINATOR: Glenn Zorpette

Recent books

Production Software that Works: A Guide to the Concurrent Development of Realtime Manufacturing Systems. *Behuniak, John A., et al.*, Digital Press, Bedford, Mass., 1992, 224 pp., $24.95.

Graphical User Interface Programming. *Rimmer, Steve,* Windcrest/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 423 pp., $24.95.

The Black Manager: Making It in the Corporate World. *Dickens, Floyd, Jr.,* and *Dickens, Jacqueline B.*, Amacom, New York, 1992, 460 pp., $22.95.

Special Functions of Mathematics for Engineers, 2nd edition. *Andrews, Larry C.*, McGraw-Hill, New York, 1992, 479 pp., $59.50.

Introduction to Random Signals and Applied Kalman Filtering, 2nd edition. *Brown, Robert Grover,* and *Hwang, Patrick Y.C.*, John Wiley & Sons, New York, 1992, 502 pp., $17.50.

Programming Tools Shareware. *PC-SIG,* Windcrest/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 336 pp., $29.95.

Object-Oriented Systems Analysis: A Model-Driven Approach. *Embley, David W., et al.*, Yourdon Press/Prentice Hall, Englewood Cliff, N.J., 1992, 302 pp., $38.

The Concise PC Notebook and Laptop User's Guide. *Gookin, Dan,* Windcrest/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 275 pp., $22.95.

Pattern Recognition: Statistical, Structural and Neural Approaches. *Schalkoff, Robert,* John Wiley & Sons, New York, 1992, 364 pp., $59.95.

Mastering Technical Mathematics. *Crowhurst, Norman H.*, TAB/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 493 pp., $24.95.

The Advanced C++ Book. *Skinner, M.T.*, Silicon Press, Summit, N.J., 1992, 288 pp., $29.95.

101+ FoxPro & dBASE IV User-Defined Functions. *Steele, Philip,* McGraw-Hill, New York, 1992, 346 pp., $22.95.

A Beginner's Guide to VAX/VMS Utilities and Applications, 2nd edition. *Sawey, Ronald M.*, and *Stokes, Troy T.*, Digital Press, Bedford, Mass., 1992, 432 pp., $27.95.

American Electricians' Handbook, 12th edition. *Croft, Terrell,* and *Summers, Wilford I.*, McGraw-Hill, New York, 1992, 1607 pp., $69.50.

Handbook of VLSI Microlithography: Principles, Technology and Applications. Eds. *Glendinning, William B.*, and *Helbert, John N.*, Noyes Publications, Park Ridge, N.J., 1992, 649 pp., $96.

Communications Wiring and Interconnection. *McClimans, Fred J.*, McGraw-Hill, New York, 1992, 354 pp., $39.95.

Circuits, Devices and Systems, 5th edition. *Smith, Ralph J.*, and *Dorf, Richard C.*, John Wiley & Sons, New York, 1992, 868 pp., $59.95.

Circuit Design and Analysis: Featuring C Routines. *Rorabaugh, C. Britton,* McGraw-Hill, New York, 1992, 229 pp., $49.95.

Food of the Gods: The Search for the Original Tree of Knowledge. *McKenna, Terence,* Bantam Books, New York, 1992, 300 pp., $20.

Internetworking and Addressing. *White, Gene,* McGraw-Hill, New York, 1992, 209 pp., $39.95.

Vision Management: Translating Strategy into Action. *Sanno Management Development Center,* Productivity Press, Cambridge, Mass., 1992, 208 pp., $29.95.

Mastering Electronics Math, 2nd edition. *Phagan, R. Jesse,* TAB/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 330 pp., $17.95.

Digital Speech Processing: Speech Coding, Synthesis and Recognition. Ed. *Ince, A. Nejat,* Kluwer Academic, Norwell, Mass., 1992, 242 pp., $75.

Innovations

(Continued from p. 11)

a bit that is about a full order of magnitude smaller.

"What most people don't realize is that the diffraction limit is not fundamental," Betzig said. Instead, it is a mathematical approximation arising from the fact that "the lens or light source is many wavelengths of light away from the surface on which you are writing."

If it were possible to hold the light source closer to the surface than a wavelength of light and if the light source has a lateral dimension much smaller than the wavelength of light, "you can beat the diffraction limit," Betzig said—a fact that had been experimentally demonstrated 20 years ago using microwaves at University College in London, he added.

In the AT&T technique, the laser light is directed not through a lens but through a tapered single-mode optical fiber of the type standard in communications systems. The taper was formed by heating the fiber and then stretching it "like taffy" into a thread until it breaks. Even though the glass is amorphous, it naturally cleaves along a flat face perpendicular to the pulling axis, forming a tapered fiber with a flat end a mere 20 nm across. The cylindrical outside of the tapered fiber is then coated with opaque aluminum, so that light injected into the wide end of the fiber can emerge only through the narrow flat tip.

Using scanning techniques developed for the scanning tunneling microscope, Betzig's team has held the tapered fiber's flat end about 10 nm from the magneto-optic material and written bits as small as 60 nm across on centers 120 nm apart. In fact, as a stunt, they lined up 100-nm bits to form the letters "AT&T," with each letter fitting inside a single bit written by the standard lens technique.

The magneto-optic material the team used is a multilayer film of platinum and cobalt, which had been developed for conventional magneto-optics. The film combines high coercivity (so that a small magnetic domain is stable) with resistance to corrosion (eliminating the need for a coating on top and allowing the tapered tip to get as close to the surface as possible).

Currently the team is focusing on ways of increasing the writing speed (now only about 10 000 b/s) and of directing the reading laser to the desired bits.

According to Betzig, the lensless technique stems from earlier work conducted at Bell Labs to perfect a more powerful optical microscope for the inspection of integrated circuits and the investigation of living cells.

COORDINATOR: Trudy E. Bell
CONSULTANTS: Ralph H. Baer, Jacob Rabinow

Calendar

(Continued from p . 7)

Visualization '92 (C); Oct. 19–23; Boston Park Plaza Hotel, Boston; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013.

Seventh IEEE Workshop on Computer Communications (COM); Oct. 20–22; Hilton Resort, Hilton Head Island, S.C.; John Spragins, 401-2 Rhodes, Clemson University, Clemson, S.C. 29634; 803-656-5907; fax, 803-656-2698.

Ultrasonics Symposium (UFFC); Oct. 20–23; Holiday Inn, Tucson, Ariz.; Vijay Nair, Motorola Inc., PRCL, 2100 E. Elliott Rd., MD EL508, Tempe, Ariz. 85284; 602-897-5922; fax, 602-897-5934.

Workshop on Power Electronics in Transportation (PEL); Oct. 22–23; Hyatt Regency Hotel, Dearborn, Mich.; V. Anand Sankaran, Ford Motor Co., Room S-2037, Scientific Research Laboratory, 20 000 Rotunda Dr., Dearborn, Mich. 48121-2053; 313-390-8689.

International Engineering Management Conference—Managing in a Global Environment—IEMC '92 (EM, N.J. Coast); Oct. 25–28; Sheraton Hotel and Conference Center, Eatontown, N.J.; Mark Troller, Stevens Institute of Technology, Department of Management, Castle Point, Hoboken, N.J. 07030; 201-216-8230.

Wafer Level Reliability Workshop (ED); Oct. 25–28; Stanford Sierra Lodge, Lake Tahoe, Calif.; Harry Schaft, National Institute of Standards and Technology, Building 225, Room B360, Route 270, Quince Orchard Road, Gaithersburg, Md. 20899; 301-975-2234; fax, 301-948-4081.

26th Annual Asilomar Conference on Signals, Systems, and Computers (SP, C); Oct. 26–28; Asilomar Hotel, Pacific Grove, Calif.; James A. Ritcey, Department of Electrical Engineering, FT-10, University of Washington, Seattle, Wash. 98195; 206-543-4702; fax, 206-543-3842.

Oceans '92 (OE, Providence, CNEC); Oct. 26–29; Marriott and Sheraton Islander Hotels, Newport, R.I.; Stanley G. Chamberlain, Raytheon Co., 1847 W. Main Rd., Box 360, Portsmouth, R.I. 02871; 401-847-8000, ext. 4423.

Nuclear Science Symposium—NSS '92 (NPS); Oct. 26–31; Hyatt Orlando Hotel, Kissimmee, Fla.; John W. Dawson, Argonne National Laboratory, Building 362—HEP Division, Argonne, Ill. 60439; 708-972-6541.

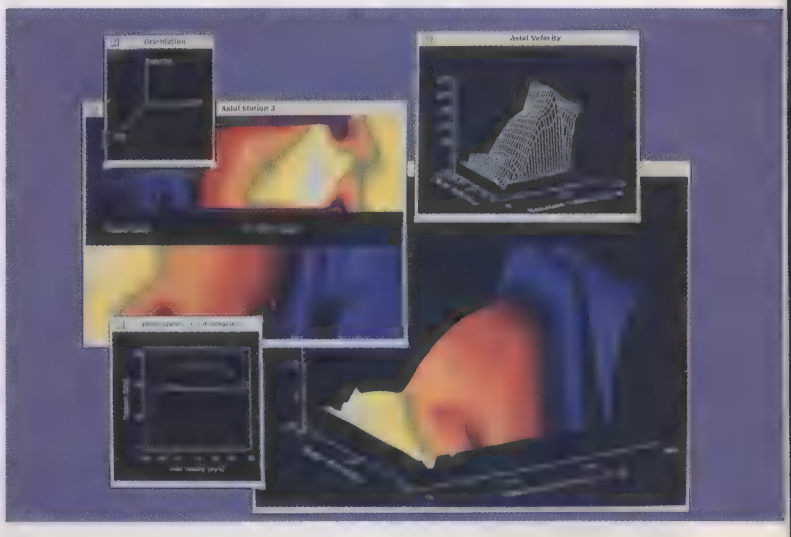
14th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMB); Oct.29–Nov.1; La Palais des Congrès, Paris, France; Swamy N. Laximinarayan, Academic Computing Center 1ST, University of Medicine and Dentistry, 185 South Orange Ave., Newark, N.J. 07103; 201-456-6007.

NOVEMBER

International Electron Devices and Materials Symposium (ED); Nov. 1–4; National Taiwan University, Taipei, Taiwan, Republic of China; W.S. Wang, Department of Electrical Engineering, National Taiwan University, Roosevelt Road Section 4, 1, Taipei, Taiwan 107, Republic of China; (886+2) 363 5251, ext. 248; fax, (886+2) 363 8247.

Regional Symposium on Electromagnetic Compatibility (EMC, Region 8); Nov. 2–5; Tel Aviv Hilton Hotel, Israel; Symposium Secretariat, Ortra Ltd., Box 50432, Tel Aviv 61500, Israel; Dani Tider, (972+3) 664 825; fax, (972+3) 660 952.

RAW. WELL DONE.



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Circle No. 32

Calendar

(Continued from p. 18)

International Conference on Computer-Aided Design (ED); Nov. 9–12; Santa Clara Convention Center, Santa Clara, Calif.; IEEE Computer Society, 1730 Massachusetts Ave. N.W., Washington, D.C. 20036-1903; 202-371-1013.

18th Annual Conference of IEEE Industrial Electronics (IE, San Diego Section); Nov. 9–13; Marriott Mission Valley, San Diego, Calif.; Robert A. Begun, 23609 Skyview Terrace, Los Gatos, Calif. 95030; 408-353-1560; fax, 408-354-1463.

IEEE Computer Society Conference on Tools with Artificial Intelligence—TAI-92 (C); Nov. 10–13; Key Bridge Marriott Hotel, Washington, D.C.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013.

Technologies Enabling Tomorrow (C et al.); Nov. 11–13; World Congress Center, Melbourne, Australia; Marg Scarlett, Convention Network, 224 Rouse St., Port Melbourne, Victoria 3207, Australia; (61+3) 646 4122; fax, (61+3) 646 7737.

IEEE Frontiers in Education Conference—FIE '92 (E); Nov. 11–15; Opryland Hotel, Nashville, Tenn.; David V. Kerns Jr., Vanderbilt University, Box 1825, Station B, Nashville, Tenn. 37235; 615-322-2771; fax, 615-343-6702.

Second Workshop on the Management of Replicated Data (C); Nov. 12–13; Monterey Marriott Hotel, Monterey, Calif.; Jehan-François Paris, Department of Computer Science, University of Houston, Houston, Texas 77204-3475; 713-749-3943.

Third International Workshop on Network and Operating System Support for Digital Audio and Video (COM); Nov. 12–13; University of California, San Diego (UCSD), La Jolla, Calif.; P. Venkat Rangan, UCSD, La Jolla, Calif. 92093-0114; 619-534-5419.

New Generation Knowledge Engineering (C); Nov. 16–18; Doubletree Washington National Airport Hotel, Washington, D.C.; Julie Walker, 11820 Parklawn Dr., Rockville, Md. 20852-2529.

LEOS '92 Annual Meeting (LEO); Nov. 16–19; Hynes Convention Center, Boston; IEEE/LEOS, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331; 908-562-3896.

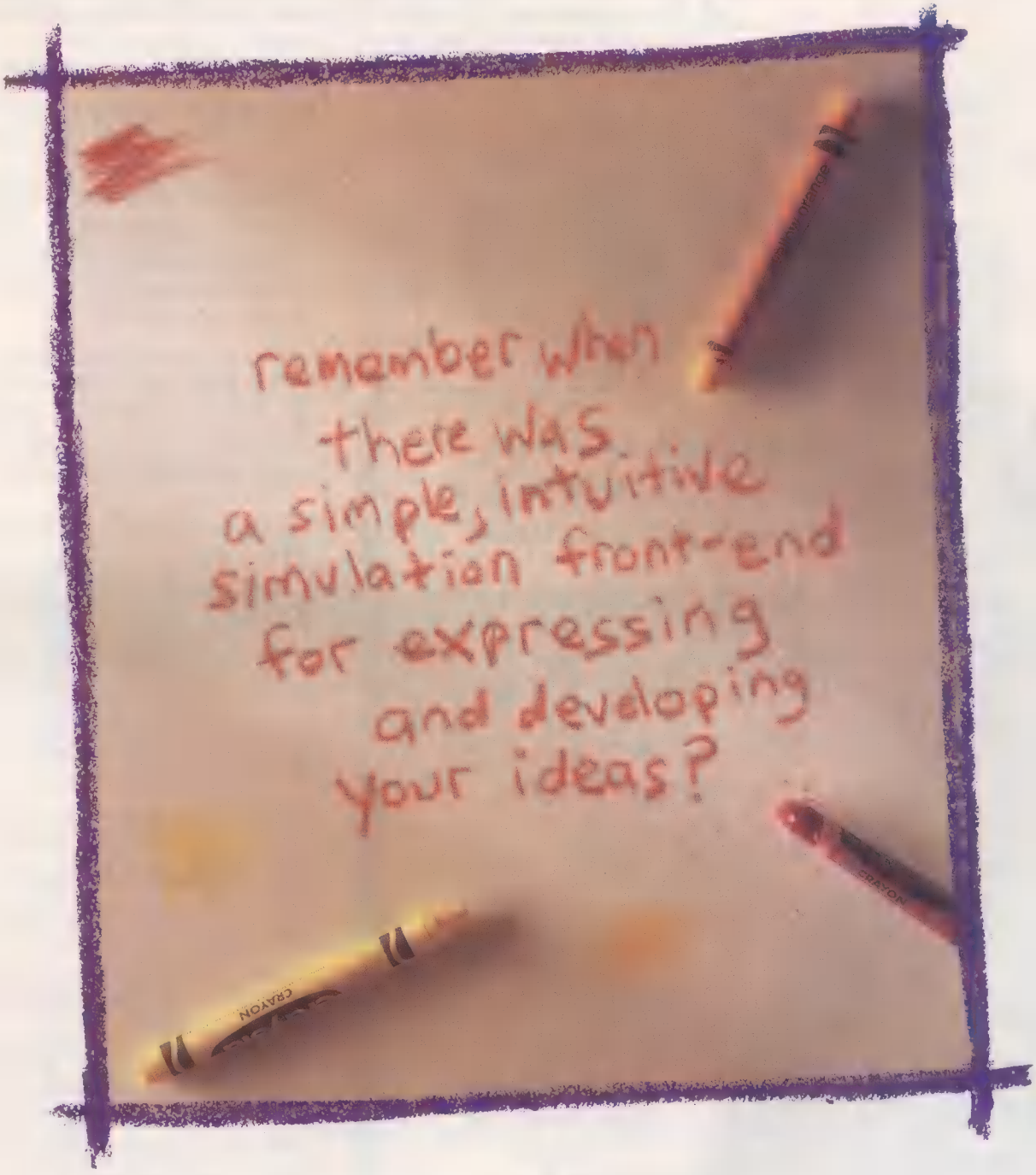
International Conference on Communication Systems/International Symposium on Information Theory and Its Applications—ICCS/ISITA '92 (IT, COM); Nov. 16–20; Westin Stamford and Westin Plaza Hotels, Singapore; Esther Yeo, Mansfield International, 71 Robinson Rd., 4th Storey, Crosby House, 0106, Singapore; (65) 224 0000.

Wescon '92 (Region 6, Los Angeles Council); Nov. 17–19; Anaheim Convention Center, Anaheim, Calif.; Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; 213-215-3976 or 800-877-2668.

Adaptive Antenna Systems Symposium (AES et al.); Nov. 19; Radisson Plaza Hotel, Melville, Long Island, N.Y.; Tom Campbell, Box 36, Greenlawn, New York, N.Y. 11740-0036; 516-757-3008.

18th Annual Convention and Exhibition—ACE '92 (Calcutta, India C); Nov. 21–23; Birla Industrial and Technological Museum, Calcutta, India; Secretariat, c/o Department of E&T.C.E., Jadavpur University, Calcutta-700 032, India; (91+72) 2851; telex, (91) 0215195.

(Continued on p. 18D)



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Circle No. 36

Calendar

(Continued from p. 18B)

First Asian Test Symposium (C); Nov. 26–27; Hiroshima Grand Hotel, Hiroshima, Japan; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

Workshop on Applications of Computer Vision (C); Nov. 30–Dec. 2; Radisson Palm Springs Resort and Convention Center, Palm Springs, Calif.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013.

DECEMBER

37th Annual Conference on Magnetism and Magnetic Materials (MAG); Dec. 1–4; Westin Galleria Hotel, Houston, Texas; Diane Suiters, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-639-5088.

Global Telecommunications Conference (COM); Dec. 6–9; Buena Vista Palace Hotel, Orlando, Fla.; Ron Kandell, Siemens/Stromberg-Carlson, 900 Broken Sound Parkway, Boca Raton, Fla. 33487; 407-955-8230; fax, 407-955-8771.

Asia-Pacific Conference on Circuits and Systems (CAS); Dec. 8–11; Hyatt Kingsgate Hotel, Sydney, Australia; Heather Harriman, IREE Executive Director, IREE Australia, Commercial Unit 3, 2 New McLean St., Box 79, Edgecliff, N.S.W. 2027, Australia; (61+2) 327 4822.

23rd Annual IEEE Semiconductor Interface Specialists Conference (ED); Dec. 9–12; San Diego Hilton Hotel, San Diego, Calif.; Lalita Manchanda, AT&T Bell Laboratories, Crawford Corners Road, M/S 4C 406, Holmdel, N.J. 07733; 908-949-1679.

International Electron Devices Meeting (ED); Dec. 13–16; San Francisco Hilton and Towers Hotel, San Francisco; Melissa Widerkehr, Suite 610, 1545 18th St., N.W., Washington, D.C. 20036; 202-986-1137.

Winter Simulation Conference—WSC '92 (C, SMC); Dec. 13–16; Crystal Gateway Marriott, Arlington, Va.; Robert C. Crain, Wolverine Software Corp., 4115 Annandale Rd., Suite 200, Annandale, Va. 22003; 703-750-3910; fax, 703-642-9634.

Conference on Decision and Control (CS); Dec. 16–18; Westin La Paloma Resort Hotel, Tucson, Ariz.; T. Basar, Coordinated Science Laboratory, University of Illinois, 1101 West Springfield Ave., Urbana, Ill. 61801; 217-333-3607; fax, 217-244-1764.

1993 JANUARY

Sixth International Conference on VLSI Design (CAS, C, et al.); Jan. 3–6; Taj Intercontinental Hotel, Bombay, India; Yashwant K. Malaiya, Computer Science Department, Colorado State University, Fort Collins, Colo. 80523; 303-491-7031; or S.S.S.P. Rao, Department of Computer Science and Engineering, Indian Institute of Technology, Powai, Bombay 400076, India; (91+ 22) 578 2545, ext. 2701 or 2714.

International Symposium on Requirements Engineering—RE '92 (C); Jan. 4–6; Hotel del Coronado, San Diego, Calif.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

International Symposium on Information Theory (IT); Jan. 18–22; Hilton Palacia del Rio, San Antonio, Texas; Galen H.

(Continued on p. 74D)

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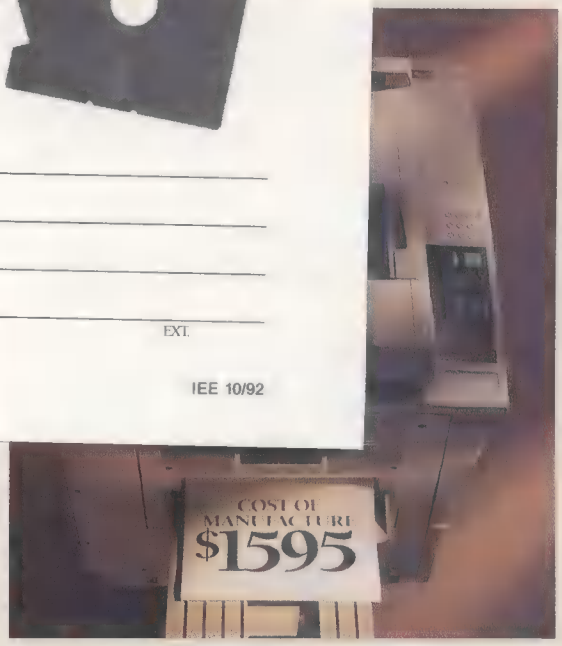
Without Design Of Experiments



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Calend

(Continued from p. 18B)

First Asian Test Sympo
26–27; Hiroshima Grand H
Japan; IEEE Computer Soc
Department, 1730 Mass
N.W., Washington, D.C. 2
371-1013; fax, 202-728-088

Workshop on Applicat
puter Vision (C); Nov. 30
son Palm Springs Resort
Center, Palm Springs, Cal

Widerkehr, Suite 610, 1545 18th St., N.W., Washington, D.C. 20036; 202-986-1137.

Winter Simulation Conference—WSC '92 (C, SMC); Dec. 13–16; Crystal Gateway Marriott, Arlington, Va.; Robert C. Crain, Wolverine Software Corp., 4115 Annandale Rd., Suite 200, Annandale, Va. 22003; 703-750-3910; fax, 703-642-9634.

Conference on Decision and Control (CS); Dec. 16–18; Westin La Paloma Resort Hotel, Tucson, Ariz.; T. Basar, Coordinated Science Laboratory, University of Illinois, 1101 West Springfield Ave., Urbana, Ill. 61801; 217-333-3607; fax, 217-244-1764.

1993 JANUARY

Sixth International Conference on VLSI Design (CAS, C, et al.); Jan. 3–6; Taj Intercontinental Hotel, Bombay, India; Yashwant K. Malaiya, Computer Science Department, Colorado State University, Fort Collins, Colo. 80523; 303-491-7031; or S.S.S.P. Rao, Department of Computer Science and Engineering, Indian Institute of Technology, Powai, Bombay 400076, India; (91+ 22) 578 2545, ext. 2701 or 2714.

International Symposium on Requirements Engineering—RE '92 (C); Jan. 4–6; Hotel del Coronado, San Diego, Calif.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

International Symposium on Information Theory (IT); Jan. 18–22; Hilton Palacia del Rio, San Antonio, Texas; Galen H.

(Continued on p. 74D)

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Circle No. 38

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Honeywell IAC, 1986

Hopi Pattern Mathematics, 6th century

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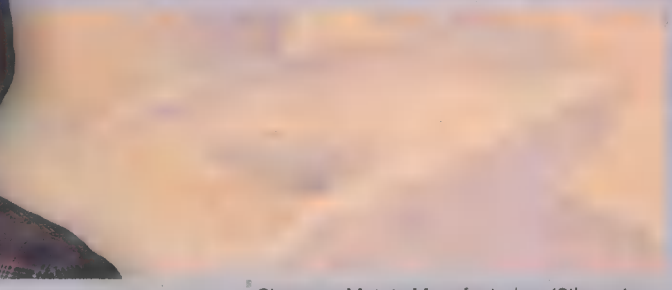
Hohokam Acid-Based Etching, 10th century

Motorola GEG, 1989

Intel, 1991



Sinaguan Metate Manufacturing, 13th century

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Circle No. 45

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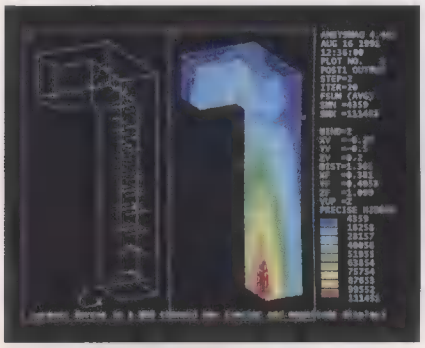
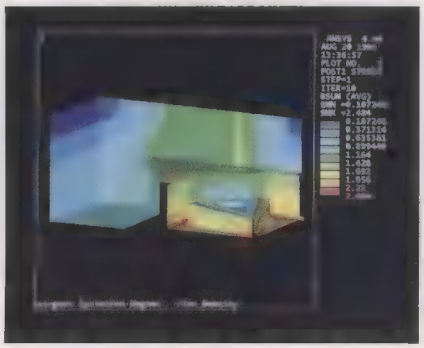
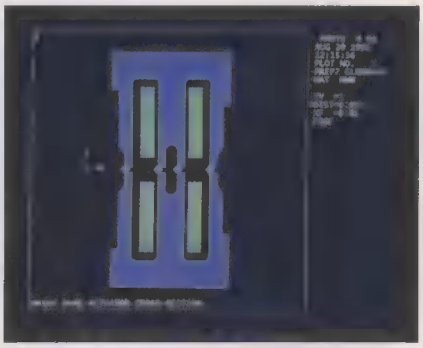


ANSYS magnetics was used by Stone and Webster Engineering Corporation with MIT Plasma Fusion Center to analyze the conductors, iron mass, and field in a MHD channel. Displayed are the Lorentz forces in a conductor.



Magnetic field analysis for a cyclotron magnet design was performed by the National Superconducting Cyclotron Laboratory, Michigan State University, using ANSYS magnetics to determine flux density levels.



A printer head linear actuator device was modeled by IBM Corporation to evaluate normal end axial forces on a sliding armature situated between two stators.

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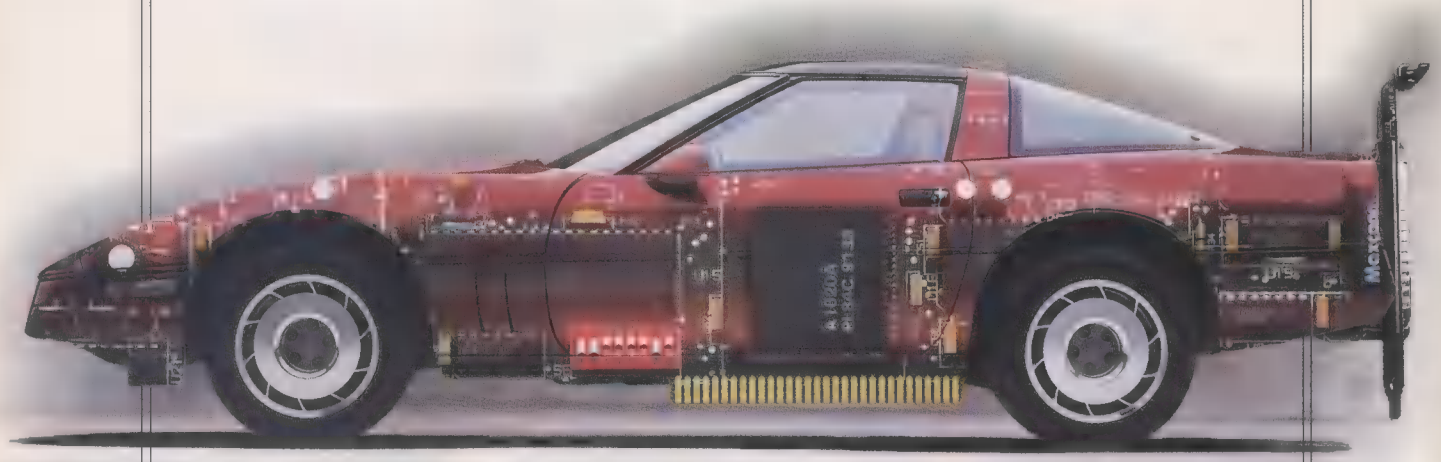

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Circle No. 34

Legal aspects

Don't lose your patent rights!

Joel Miller

After months of effort, you've finished the development of an improved power supply circuit for notebook computers. Everyone who has seen the device was impressed—they've all said that there is nothing like it on the market. Moreover, at last year's IEEE meeting, your presentation describing the circuit in detail was well received. At the urging of your colleagues, you go to see your company's patent attorney to investigate patent protection.

After relating your successes and the encouragements of your co-workers to the attorney, you learn that the prospects for a patent are slim, because you may have inadvertently waived your rights.

How could this have happened? What could you have done to avoid it?

KEEP IT UNDER YOUR HAT. In the United States, if an invention is publicly disclosed more than one year before ■ patent application is filed, one is not entitled to the patent—the invention is considered to be in the public domain. Public disclosure can be a sale, an offer for sale, a demonstration at a trade show, or a magazine article describing the invention. If an invalidating public disclosure is not caught, it may well surface during litigation since an accused party has great incentive to root out evidence that could undermine an asserted patent.

Moreover, premature disclosure can severely jeopardize non-U.S. rights. While the inventor may enjoy ■ one-year grace period in the United States, many countries—including Belgium, Greece, Great Britain, Spain, and Taiwan—require absolute novelty. Any disclosure before the filing of a patent application will bar rights to a patent. If you contemplate obtaining patent protection in countries outside of the United States, you must file before engaging in any activity that constitutes public disclosure.

WHO'S ON FIRST? Besides the problems associated with an inadvertent disclosure, an inventor should recognize that others may be out there working on the same problem. In the event that more than one person applies for a patent on the same invention, the patent office will have to determine who is entitled to the patent.

In most countries, such as Japan, that determination is relatively straightforward: generally speaking, the first person to *file* a patent application is considered to be the inventor. In the United States, however, a person who is diligent in perfecting the invention and pursuing protection, and who can prove that he or she invented the device before one who filed first, will be awarded the patent—even though that person filed later. Thus, in the United States, the first person to *invent* will be awarded the patent.

How do you prove that you were first? Many inventors operate under the mistaken assumption that they can establish ■ date of invention and protect their ideas simply by placing a description in an envelope and mailing it to themselves, a concept that has become firmly rooted in the folklore of patents. Unfortunately, such a tactic is far from conclusive in determining priority.

The applicable statute and the relevant court decisions require corroborated evidence—that is, it must be witnessed by ■ knowledgeable person. A colleague should read the relevant portions of the inventor's laboratory notebook and then sign his or her name under the legend "read and understood" and date the notation, ideally on each page of the notebook. This process should occur on a regular and frequent basis. If the notebook is on a computer, print out the day's work and have it witnessed.

If the application's priority is contested, the inventor may be required to submit evidence of priority. A well-documented record will help to establish just what was developed and when those developments occurred. Without the aid of a properly witnessed notebook, this task will be considerably more difficult.

The penalty for not keeping ■ complete and accurate record can be high. In one of the best-publicized cases in engineering, a graduate student named Gordon Gould began conducting experiments on light amplification devices in the late 1950s. Although Gould was ultimately credited with some of the developments in the field, he was unable to establish an early claim to the laser.

After several years of legal proceedings, a Federal appeals court in 1966 upheld the award of patent on the laser to Bell Telephone Laboratories employees Arthur L. Shawlow and Charles H. Townes instead of Gould, because he was unable to prove that his efforts preceded theirs.

Gould's loss was due in large part to his failure to properly document his work, a not-uncommon problem in the engineering world. When pressed to show that he had developed the laser before his opponents had, all that Gould could offer were incomplete notes witnessed by a notary public, "too ambiguous to justify the conclusion that [Gould] possessed 'a definite and permanent idea of the complete and operative invention.' " Not being technically skilled, the notary could neither evaluate nor understand the notebook. Thus, Gould was without adequate support for his claim.

Although the United States may likely change to a first-to-file system of priority as part of an international effort to harmonize patent protection for industrialized nations, there may still be circumstances where it is necessary to establish priority of invention.

There are additional reasons for keeping accurate records of development. In large companies, it is not unusual to have several people collaborating on a project, sometimes leading to confusion over which names should go on ■ patent application. Laboratory notebooks can help to identify the correct inventors. Also, should your company be accused of misappropriating trade secrets, an entry in a notebook showing that your company possessed this information before your opponent could save much aggravation and perhaps cut short a legal proceeding.

FILE NOW, PLAY LATER. The urge to tell others about ■ new design and commercially exploit it is irresistible. However, doing so before filing ■ patent application can lead to difficulties, if not a complete loss of rights.

If you think that you might be interested in patent protection, the best course of action is to obtain advice early. Carefully document your work as you go along and have your notes properly witnessed. If you are planning to deliver ■ presentation during which you will be discussing your invention or should you wish to display the product, don't procrastinate: when you have completed the invention, have an application prepared and filed without delay.

Joel Miller is an attorney in private practice in West Orange, N.J.

COORDINATOR: Trudy E. Bell

Spectral lines

OCTOBER 1992 Volume 29 Number 10

Challenges to management

"Scientific management" grew from an attempt beginning in the late 1800s by mechanical engineer Frederick Taylor and his followers to instill in factory workers a more friendly and cooperative attitude toward management, so that they'd produce more product. He did this by establishing systematic tasks for workers and bonuses for bettering standard production rates.

Taylor evidently had mixed feelings about the factory worker. On the one hand, he thought the average worker to be inherently lazy. "There is no question that the tendency of the average man (in all walks of life) is toward working at a slow, easy gait, and that it is only after a good deal of thought and observation on his part or as a result of example, conscience, or external pressure that he takes a more rapid pace," he wrote in 1911.

On the other hand, he observed that management helped ingrain such habits into the worker by setting piecework pay rates too low, or by decreasing them if a worker consistently beat the standard expected output.

Taylor also decried the "herding" of workmen into "gangs." Loss of ambition and initiative is fostered if they are not treated as separate individuals, he said. Even at Bethlehem Steel, where up to four men were allowed to work together in a gang, each laborer wherever possible was given a "separate individual task," Taylor noted.

Although one of his principles of scientific management was "the scientific selection and training of the workmen," whatever industry did in this regard during Taylor's active career was primitive in comparison to subsequent practices of personnel screening and training.

Generations later, the setting of standard methods for factory tasks by industrial engineers (part of scientific management) gave way, selectively, to more participation by the workers themselves in how a product should be put together, or who should do it. This innovation gained popularity in instrument houses producing larger, more complex, and comparatively low-volume products.

Even later came "quality circles," first in Japan and then in the United States, in which both workers and managers were encouraged to trade ideas concerning ways to produce a particular product more efficiently and at a higher quality level. Little documentation exists on the relative participation by individual members of quality teams, or how such teams affect "every man's desire for a larger income," as Taylor's compatriot Frederick Halsey defined the essential factor in systematic management of factory workers.

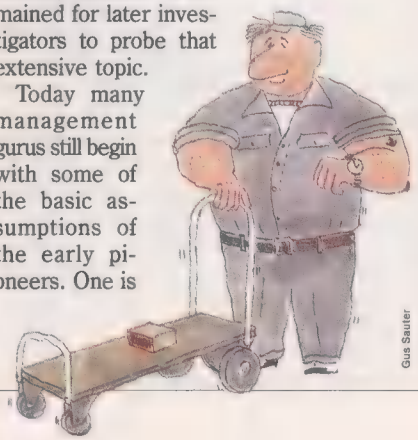
Quality circles are related to the contemporary concepts of self-actualization and empowerment, and to the notion (limited in practice) that all workers in a department should learn each other's jobs. However, many of these experiments and ideas are inconsistent with the traditional principles of Taylor's scientific management, and in particular with the notion of task specialization.

In any event, in Taylorism, the assumption was that managers would manage (and think) and workers would work (and not think). Not much attention was given to the process of upgrading workers to managers. Even more important, scientific management ultimately demanded a new element in the factory—a professional level of industrial engineers—to determine factory layout, methods, and production rates.

Does scientific management, as it has evolved today, play any role in industrial management aside from the factory floor? Taylor himself excused a minority of employees from his blanket epithet of "lazy." He spoke of "men of unusual energy, vitality, and ambition who choose the fastest gait, who set their own standards, and who work hard . . . ." Quite possibly he had in mind some of the managers and engineers of his day.

But the applicability of the traits of factory workers—so assiduously analyzed by Taylor and his converts to scientific management—to managers and engineers is scantily treated. It remained for later investigators to probe that extensive topic.

Today many management gurus still begin with some of the basic assumptions of the early pioneers. One is that because managers and workers have different interests, they make up fundamentally two classes of human beings.



Gus Sauter

Of course, there *are* some notable differences. Hourly workers generally rate take-home pay as the No. 1 job consideration. Managers, engineers, and other professionals often do not. Nevertheless, there's little doubt that all employees, from the most menial to the CEO, count as important the psychic rewards and social relationships stemming from their jobs.

At the other extreme, those who postulate that all employees—whether factory or office hourly, management or professional—have nearly identical job concerns, are themselves misled. For example, it is overly optimistic to assume that all members of a quality circle benefit from their participation. Some workers still want only to know what is expected of them at their workstation, what they'll be paid, and what the working hours are.

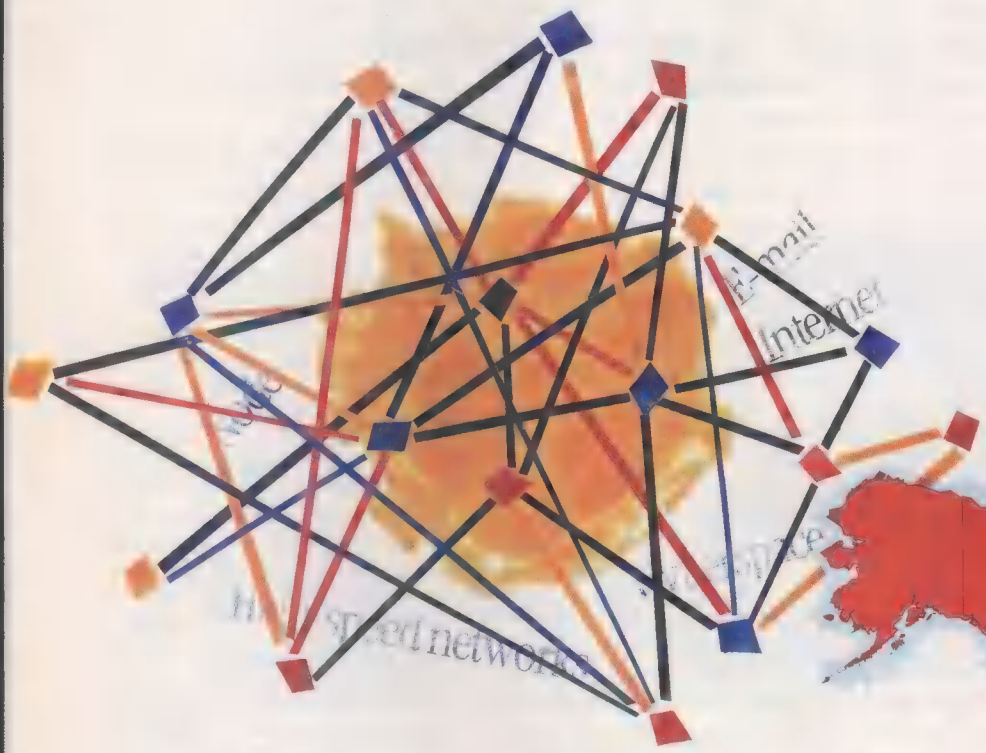
Likewise, not all engineers and managers are encouraged by the prospect of moving progressively from R&D through the design and production cycle and on to customer engineering or sales. Nor are all professionals excited about the interdepartmental communication that the new concept of concurrent engineering demands. Forced to attend meetings and seminars to broaden their knowledge about other functions of the corporation, they fret about losing time that could be beneficial in doing their "own" job better. And they sense an inefficiency in the democratic process of decision-making.

Still, there are accelerating factors that today demand greater flexibility of employees at all levels and suggest a need to broaden their knowledge beyond their current job. Among them are the trying economic environment, global competition, pressures to convert from military to commercial products, and concomitant workforce reductions.

Managers are hard pressed to select among time-honored management techniques and current management fads to provide a self-consistent management process. Meanwhile, the uncertainty of corporate directions and even entity survival makes the job of providing credible management and instilling some degree of employee loyalty a sometimes insurmountable challenge.

Donald Christiansen

E-MAIL
PERVASIVE AND PERSUASIVE



The net of networks now embracing the globe is bypassing corporate and other hierarchies

Mail service is the nervous system of nations and empires. From message runners in ancient Greece to the Pony Express that coupled the wild west with the eastern United States, the speed of message delivery has wrought dramatic changes in societies. Today computers hitched by globe-girdling communications lines link a domain that is freed of time, distance, and political boundaries, made possible by electronic messages that travel over speed-of-light highways.

For example, a U.S. resident cannot make a phone call to Cuba or travel there directly: the U.S. government blocks such routes. But if the person knows a Cuban's electronic name and address (a sometimes cryptic series of letters and symbols), he or she can send messages there with a couple of keystrokes at the cost of a local phone call. For that same local call, his computer can connect him to peace activists in Central America or supercomputer specialists in Russia. Nor is it unusual for engineers in Scotland to use an e-mail network to collaborate on designs with colleagues in New England, California, and Israel.

Such is the power of the net. Still nascent, it already encircles most of the globe [see map]. It resists control by governments or any central authority, perceiving attempts at censorship as electronic malfunctions and reconfiguring itself to avoid them. Thus, it is a force for democratization of governments and social change [pp. 30–33]. In fact, it may have played a role in subverting last year's attempted coup in the then Soviet Union.

The network is blind to race, age, gender, or handicap. As a new source of leisure-time fun, it includes social opportunities for the

Tekla S. Perry Senior Editor
(tekla@well.sf.ca.us)
John A. Adam Senior Associate Editor
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housebound and personalized news services for everyone [p. 29].

It is also transforming the workplace. Engineers quitting for the day pass design problems over time zones much like a baton in an endless relay race; companies call upon researchers separated by oceans to collaborate on complex projects [pp. 24–28]. Corporate e-mail is breaking down hierarchies by making upper managers more accessible and speeding up the pace of research.

Electronic mail evolved spontaneously in various computer timesharing systems in the mid-1960s. "It was fairly obvious in timesharing that leaving messages for other users would be convenient," said Frank Heart, senior vice president at Bolt, Beranek, and Newman Inc. (BBN), Cambridge, Mass. These early mail systems were casually written, often as a weekend project by a programmer or two, and had no uniformity.

Then in 1969, the Advanced Research Projects Agency Network (Arpanet) was begun by the U.S. government so that researchers at universities and other facilities might electronically ship computer data to each other and remotely launch computer programs.

A year later, Raymond Tomlinson, a principal scientist at BBN, the main Arpanet contractor, wrote ■ program employing Arpanet's file transfer protocol. The software let BBN's local mail system communicate with independent mail systems at the other Arpanet sites. The result: e-mail quickly became a key means of communications between Arpanet users, as well as ■ vehicle for transmitting other information such as executable programs and data files, packaged as e-mail messages.

Today e-mail reaches many millions of people around the globe, from New York City to Tokyo and Siberia to the Vatican. Various networks continue to grow exponentially, even though e-mail itself has been constrained by incompatibilities ["Meta-matrices," pp. 26–28]. For instance, ■ person connected to seven networks—like Compuserve, GEnie, FidoNet, MCIMail, the Well, Unix-to-Unix Copy, and Bitnet—may need seven addresses because gateways between networks have been slow in coming. Addresses for messages that cross networks are complex—and some are incredibly lengthy.

All this activity on the network has raised concerns over privacy ["Data Security," *IEEE Spectrum*, August 1992, pp. 18–44] and also over the complicated and somewhat unclear legal protections for information "published" on ■ computer network [a topic to be addressed in ■ future *Spectrum* article].

Obviously, e-mail masks out many of the cues present in other forms of communication—body language, voice inflection, even the stationery (business letterhead, monogrammed notes, or scented tissue) that gives paper mail a personal touch. To compensate, it has developed its own language of images. Read by being mentally turned 90 degrees clockwise, these "emoticons" or "smilies" inflect messages in ■ host of ways. A few examples:

:-) A joking comment
;-) A flirtatious or sarcastic comment
:-(A frown, the user is upset or depressed
>:-< Even madder
>:-> A devilish remark
:-D A laugh
:-@ A scream
%-) Confused
:-X My lips are sealed
:* A kiss

Improvements in electronic mail services are on their way. While the e-mail world is still somewhat biased toward the *avant-garde* technical elite, commercial users are hooking up in droves, creating a demand for easy-to-use services. According to George Cunningham, vice president of product planning at AT&T Easylink Services, Parsipanny, N.J., e-mail by the mid-'90s will take off in the consumer realm. Portable notebook computers with built-in wireless modems will enable users to send and receive e-mail anywhere.

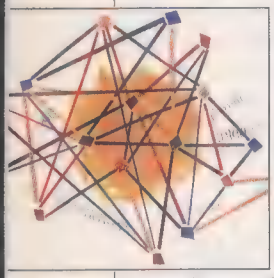
Perhaps the biggest initiative on the e-mail horizon is the planned high-speed National Research and Education Network (NREN). The multibillion-dollar U.S. endeavor is to lay down gigabit-capacity links that will allow more bandwidth-intensive graphics and video to be included with text and voice. It is to link more than ■ million computers in all 50 U.S. states for use by high-performance computing researchers, and is expected to boost other consumer and business network services as well.

BBN's Heart has his own view of being hooked up, one that millions more may soon agree with. "E-mail," he said, "is like a clothespin. Once you figure it out, you can't hang your clothes without it." ◆

Most of the world, 108 countries so far, is connected to electronic networks. At the low end [C], these nets offer at the very least electronic mail services, while those at the higher end [A] have the ability to transfer files and to remotely log-in to, say, supercomputers. Information on former Soviet republics may be incomplete, but otherwise data is current to Aug. 31; it was compiled by Larry H. Landweber, professor of computer sciences at the University of Wisconsin, in Madison.

E-mail at work

Electronic mail has removed the barriers of time and place between engineers collaborating on complex design projects



Recently, 53 engineers at Digital Equipment Corp.—spread across Massachusetts, Arizona, Colorado, Singapore, and Germany—collaborated on the design of a new disk drive. Most had never met and phoned each other rarely. Yet Digital estimates that this dispersed group finished its project one year sooner and needed 40 percent fewer people than would have a team assembled in one building. Another recent project at DEC, the Alpha chip, an integrated-circuit design, also made effective use of e-mail by calling on engineers in Israel, Massachusetts, and Scotland.

Tandem Computers Inc., Cupertino, Calif., has a similar tale. In June the company announced a central office switching system for use with the SS7 telephone network. The 40-some engineers on that project were scattered among five buildings in California and two in Texas. The project manager called the lead engineers at each location only once a week and visited those sites only a few times a year; yet the scattered designers worked as a cohesive unit.

Electronic mail networks that reach virtually every employee make such geographically distributed work teams commonplace at DEC, Maynard, Mass., and Tandem as well as at other engineering companies.

"Every new employee at Tandem gets an ID card and a mail access code," said David Foley, network architect there. "And they may have the mail access several days before the ID card."

At DEC, said Peter E. Brown, corporate telecommunications manager, "the first thing we all do when we get to work in the morning is check our electronic mail."

Companies that have come to rely on electronic mail have huge international networks. Palo Alto, Calif.–based Hewlett-Packard Co. has a network of 94 000 mailboxes (some dedicated to groups, others to individual subscribers), which delivers over 350 million messages every year to its 90 000 employees. DEC's network sends 110 000 employees around 50 million messages annually between sites (intrasite mail is not included in this tally).

Tandem's net links 11 000 employees and delivers about 60 million messages a year. At Sun Microsystems Inc., Mountain View, Calif., the network has 12 500 users.

These systems support different flavors of electronic mail. Private e-mail is person to person, and can comprise computer-aided design files and digitized images as well as text. Wide-distribution e-mail originates with one person but is sent to many and replaces interoffice memos. Electronic conferencing allows users to identify topics—often technical, but in some cases with as little connection to work as movie reviews or softball scheduling. Anyone may review a running transcript of a conference and append a comment.

Engineering managers interviewed by *IEEE Spectrum*, an admittedly unscientific sample, typically receive about 25 messages daily; engineers receive more or less, depending on the intensity of projects they are working on and how many interest groups they belong to.

So far, though engineering organizations like these large corporations are at the leading edge of e-mail usage, others, particularly small companies, have decided that they have little need for electronic mail.

> A person. . .can say 'Help' to 10 000 people. . . The next morning he may have 15 answers to the problem

Electronic mail is also in less use in some fields, noted Rob Kling, professor of information and computer science at the University of California at Irvine. For example, aerospace engineers are seldom network users.

However, engineers and scientists are pioneers in electronic mail use, and professionals in other industries are following suit in growing numbers: at the Fortune 2000 corporations, some 11.7 million workers are e-mail users, and that figure is expected to grow to 27 million by 1995, according to a recent study by the Electronic Mail Association, Arlington, Va.

COMPETITIVE EDGE. The advantages of electronic mail are many. Besides the obvious boon of avoiding telephone tag and time zone dissonance, e-mail gives companies unprecedented flexibility. Managers can assemble engineering teams by tapping the best people for the project without concern for their location, then disband them as soon as the project is done. Electronic mail also eliminates the need for stressful transfers or expensive temporary assignments.

In fact, some companies have discovered that the time-honored method of assembling a multifunctional team either from employees at one site or by means of transfers or regular meetings is no longer practical. According to a study conducted last year by David Cedrone, DEC's corporate voice and video manager, and Edward McDonough, a professor from Northeastern University in Boston: "As projects become increasingly complex and greater numbers of uniquely skilled people are needed on project teams, more and more time will be needed to gather them together in a common location."

This flexibility may let companies operate with a smaller workforce—a specialist, say, may work part-time with two project teams many hundreds of kilometers away. Also, interdisciplinary teams may crop up more—a group might not need a full-time cabinet designer for its project, but would jump at the opportunity to bring one onto the team part-time, instead of tossing a finalized design to the cabinet department. "Many individuals are required in 'bursts,'" Cedrone and McDonough concluded in their study. "Full-time assignment of individuals rarely matches the real resource demands of a project."

Electronic mail can also uncover hidden expertise in a company. When a design team at a networked company runs into a problem that stumps all team members, it broadcasts a "does anybody know" request throughout the network, and suggested solutions often appear in a matter of hours. James Treybig, president of Tandem, has said that "a person in Switzerland on electronic mail can say 'Help' to 10 000 people (which a person cannot do on the telephone).

Tekla S. Perry Senior Editor

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The next morning he may have 15 answers to the problem, of which 13 are wrong. But he has answers."

A study at Tandem by researchers Sara Kiesler, Lee Sproull, and David Constant of Carnegie Mellon University in Pittsburgh found that during a six-week period, employees broadcast about seven questions a day that elicited about eight replies each. The great majority had first tried and failed to find solutions using other sources. Some of these replies went into open reply files that could be accessed by other employees with similar questions.

Another Tandem study done by Tom Finholt, now assistant professor of organizational psychology at the University of Michigan, Ann Arbor, found that the reply files were accessed more than a thousand times a month. The engineers who used this database most were those farthest from Tandem's California headquarters.

For some companies, electronic mail has meant the ability to tap into expertise that would have been completely inaccessible without it. Report Cedrone and McDonough in their study: "Pockets of expertise and specialization exist throughout the world."

At Sun Microsystems, engineers are collaborating with a team of 33 former supercomputer designers in Moscow, St. Petersburg, and Novosibirsk to develop compiler software for Sparc workstations, to be marketed in the United States, Europe, and Japan. Because the telephone network in Russia is unreliable, and most of the Russian designers have difficulty with spoken English, electronic mail is for many project workers the sole means of transatlantic communication. It is used to debate complex technical issues as well as deal with more mundane problems. (The California engineers helped their Russian counterparts network their workstations after the Russians e-mailed a file in PostScript, a printer language, that contained the floor plan of their office building.)

Project teams that span time zones may speed development by working round the clock. Hewlett-Packard has research laboratories in Bristol, England, and Tokyo, as well as in Palo Alto, and joint projects are becoming common. "The time difference means [the overseas] engineers are going home as we are going to work and vice versa," said David Ricci, director of research services at Hewlett-Packard Laboratories in Palo Alto. "So we can leave them a message at the end of our day, and they can pick up and work where we left off, then hand it back to us in our morning."

"Electronic mail gives us about a 30 percent gain in productivity," estimated David Ditzel, director of advanced development at Sun.

In discussing a study of electronic mail usage in a number of software design organizations, Carnegie Mellon researchers Sproull and Kiesler write in their book *Connections: New Ways of Working in the Networked Organization*: "We discovered a very high correlation between use of electronic mail and group productivity."

Electronic mail also leads to increased communications by engineers in the same building, even in adjoining offices. The reason, pointed out Jan Walker, a member of the research staff at DEC's Cambridge Research Laboratory, is that electronic mail is not as intrusive as a phone call. It does not interrupt the recipient, and for the sender, takes less time since he or she need not run through the social amenities. "Getting eight phone calls would be disruptive when you are in the midst of something, but receiving eight e-mail messages is not, and often you can answer with just a yes or a no," Walker told *Spectrum*.

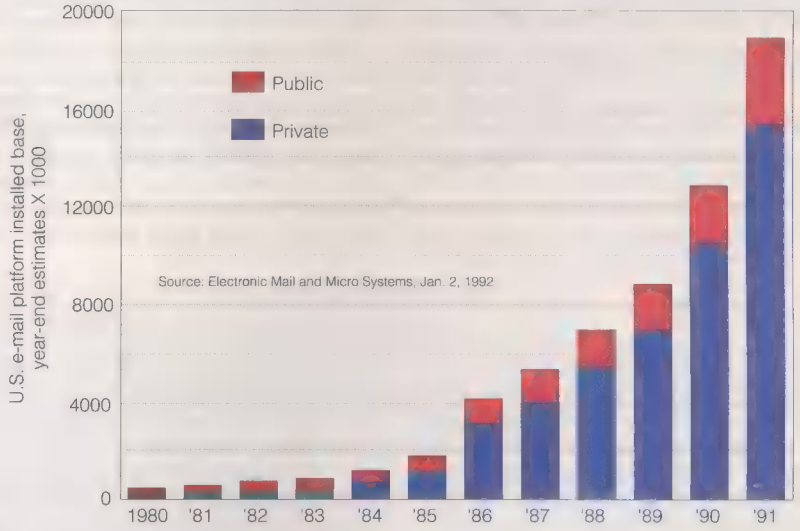
A fringe benefit of communicating electronically is that a record is kept of all conversations. Meeting "notes" can be distributed to interested parties outside the core team, new team members can easily review past discussions and get up to speed, managers can review the reasoning behind a decision, and a message received by one person can be forwarded easily to others.

"We go back quite often and refer to old messages for part numbers or specs," said Glenn Rankin, a development engineer at HP. "It doesn't require writing things down and putting them in a notebook somewhere."

Finally, perhaps least in importance, though not trivial, e-mail is a bargain. According to Hewlett-Packard's calculations, a two-page electronic mail message between any two HP employees worldwide averages US $0.22; a letter averages $0.51, and a fax averages $1.66.

Studies have shown, however, that e-mail does not reduce travel very much. Robert Lucky, executive director of research at AT&T Bell Laboratories, Murray HIll, N.J., noted that e-mail makes it even easier to go on the road because the traveler does not risk losing touch with his or her colleagues. And engineers still subscribe to technical journals to track developments in their fields. In fact, according to research by Starr Roxanne Hiltz, professor of sociology at Upsala College, East Orange, N.J., e-mail users tend to read more, rather than less, probably because associates send e-mail messages referring to published articles.

But does e-mail really allow distant colleagues to work as closely together as they would if they were not geographically separated? The engineers who use it say it does, though sometimes it takes a little creativity to communicate clearly. At DEC recently, engineers were trying to launch the manufacturing in Augusta, Maine, of a new digital router (a dedicated device for directing data communications traffic) but were stymied by defects, so they sent an oscilloscope trace to peers in Clonmel, Ireland. The Irish engineers responded the next day: you must be using capacitors from such and such a vendor, replace them and your problem is solved. It was.



The number of private U.S. electronic mail networks installed by corporations, nonprofit associations, and universities [blue] has grown much faster than their public counterparts [red].

ENDING ISOLATION. The earliest users of electronic mail were researchers at universities. Since the Advanced Research Projects Agency Network (Arpanet) provided the first reliable electronic highway in 1969, communication over the net has accelerated the process of research.

Researchers thousands of kilometers apart meet in on-line discussion groups devoted to their specialties, and communicate regularly on the net with peers whom they may never have met.

"One of the facts about being an expert in something and working at a university is that a typical university can't afford to maintain more than one or two experts in a field on staff; therefore, experts tend to be spread all across the globe," said psychologist John Condry, a professor at Cornell University in Ithaca, N.Y. "But with e-mail, I talk regularly to a dozen people who are doing the same research I am, communicating as ef-

fortlessly with people in France, Sweden, and Israel as next door. By forming nodes of interaction, e-mail may well speed up the process of science."

Sociologist Hiltz's research on the use of electronic mail by scientists confirms this conclusion. "Perhaps [electronic communication] is like an intellectual lonely minds club," she writes, and indicates it has probably had its biggest impact on those at the smaller universities. The scientists in her study reported more communication with both people in their fields and those in other disciplines that resulted in productivity gains by "increasing the stock of ideas and providing leads, references, and other information."

"Subjectively experienced effects of the increased communication with a larger network of scientists include the ability to get 'instant feedback' on ideas and to 'kick ideas around' with others when a piece of work is in its formative stage," Hiltz writes.

With e-mail, months or years no longer pass between a researcher's completion of experiments and the dissemination of results. Now, scientific papers are "published" on the network, commented on, and often revised and "republished" several times before they appear in traditional journals or are delivered at conferences.

> By forming nodes of interaction, e-mail may well speed up the process of science

Sometimes the pace of net vs. journal publication trips over itself. A paper finally published in a journal in, say, September may reference a paper to be published in the same journal in November, since the electronic forms of both papers had already been widely circulated and seen by both authors.

Some think e-mail may have dramatically sped the response to the purported demonstration of cold fusion claimed by Stanley Pons and Martin Fleischmann in March 1989. Information about their results was distributed on Bitnet, a worldwide academic network, before it was published in a journal; comments by other researchers, from quick responses to detailed reports of attempts to replicate the experiments, followed on the network and in a flurry of faxes between universities.

Writes Frank Close in *Too Hot to Handle*, an account of the cold fusion announcement and its debunking: "By Monday afternoon [the day after cold fusion was announced in a press conference] information was coming in by phone, fax, and Bitnet. A new genre in scientific communication was being born. You logged in at any time and read the latest gossip or hard news and sent in any insights you had gathered yourself.... The 'paper'— really a set of electrical signals propagating through the air—flashed round the world like an electronic chain letter."

According to Richard Petrasso, a principal physicist at the Massachusetts Institute of Technology (MIT) in Cambridge, electronic mail discussions backed up by preprints of papers and errata transmitted by fax "had a direct impact on our work," leading to the publication of several papers on the topic shortly after the cold fusion experiments were announced.

Nate Lewis, a professor at the California Institute of Technology in Pasadena, said researchers in his cold fusion group "read

Meta-matrices

"Uncontrollable" is the best way to describe the growth of big networks, said Vinton Cerf, president of the recently formed Internet Society, and a computer scientist at the Corporation for National Research Initiatives located in Reston, Va. No one really knows just how extensive many of these decentralized computing webs of cyberspace are. The indicators are, however, that the proliferation is occurring exponentially.

A half-dozen varieties of wide-area networks exist. Besides the many commercial offerings such as Prodigy and CompuServe [To probe further, p. 33], there are the exchanges for science, technology, and education. The Internet is the largest all-purpose global meta-network supported by governments, while FidoNet represents another class of connection, the kind formed spontaneously by individuals without much investment.

INTERNATIONAL NET. The Internet traces its origin to Arpanet, a computer science experiment set up by the Pentagon's Advanced Research Projects Agency in the late 1960s. In the next decade, Arpanet's growth plus a confluence of terrestrial and satellite switching technologies and the development of local-area networks set the stage for wide-area interlinked computer networks.

An additional influence came from the U.S. Department of Defense, which in 1978 endorsed the Transmission Control Protocol/Internet Protocol (TCP/IP) as a data communications standard. Devised in part by Cerf, then at California's Stanford University, TCP/IP in 1983 was made a requirement on Arpanet and Milnet, a Government military network, by the Defense Communications Agency.

After that, companies responded by making TCP/IP-compatible products, like routers and modems. "That was the beginning of the explosive period of growth," Cerf told *IEEE Spectrum*.

The Internet protocol suite, now widely accepted internationally, is designed for decentralized use and to link heterogeneous systems. The collection of networks that share this protocol is known as the Internet.

Once hooked on to the Internet, most users pay no more to send 1000 messages to Tokyo than to send 10 to Boston. Lower-echelon users are generally charged a one-time installation fee of several thousand dollars for a dedicated phone line and telecommunications gear. Cyndi Mills, manager of NSF Network Services (NSFnet), Cambridge, Mass., and head of the Internet Engineering Task Force's accounting working group, said rates vary from $25 to thousands of dollars a month, according to how much bandwidth is rented and the size of the organization.

FLOWING TRAFFIC. The Internet is analogous to a highway system, with dedicated communications links—copper and glass fiber cables as well as satellites—functioning as the concrete and asphalt. Leased phone lines of 56 kilobits to 1.5 megabits per second often serve as the on-ramps, connecting to regional networks. The capacity of the T1 highways is 1.5 Mb/s; that of the T3 routes is 45 Mb/s. These latter are currently being installed by a nonprofit joint venture by IBM, MCI, and Merit Network called Advanced Network and Services Inc., located in Elmsford, N.Y.

Breaking messages into various sizes of packets, which are then sent along optimum routes, helps to keep traffic flowing and to make efficient use of the expensive high-capacity links. Though gigabit-per-second superhighways are still in the research stage, they will be essential for bandwidth-intensive imagery. (Recently the MIME Internet standard for sending multimedia e-mail was completed. In July, during a technical conference, voice and images using the MIME standard were sent over the Internet to several countries.)

About 17 000 networks now plug into the Internet, and its users number in the millions. According to a quarterly survey done in July by Mark K. Lottor, a consultant for the network information systems center of SRI International, Menlo Park, Calif., the Internet has 992 000 host computers, up by 100 000 since April.

Data on the NSFnet from Merit Network Inc., Ann Arbor, Mich., show how the largest backbone of the Internet is used. In June, 15.7 billion packets were transmitted on NSFnet, more than double the number of June 1991 and five times that of June 1990. File exchanges accounted for 31 percent of the usage; electronic mail, for 21 percent; and interactive computing such as telnet (where a user logs in remotely to operate, say, a supercomputer), for 13 percent.

NSFnet is truly international. Over and above the 3898 networks in the United States linked to it, as of July 1992 NSFnet had a total of 30 networks in Brazil, 3 in Estonia, 10 in Poland, 119 in Japan, 187 in the United Kingdom, 287 in Germany, 243 in France, and 253 in Canada.

Like postal and highway systems, Internet receives subsidies from assorted government agencies for research, installation, maintenance, and service help. Consequently, the cost of a single message is "vir-

the latest gossip" on the networks every day. "It propagated rumors, but it also kept close track on the facts."

A drawback of electronic mail, though, is that the ability to move fast is not always positive. "Anytime there is a rush, there is less time to contemplate your results," said Petrasso at MIT. "A scientist needs time to cogitate about his paper. We all make mistakes, and the increased rapidity in communications is depriving the scientist of the time to think, and talk to colleagues, and change things before they are made public. As a consequence, there will be more mistakes committed by scientists; maybe because of e-mail the mistakes will be discovered more quickly by others, but it doesn't make it a happier environment."

These days, however, said Lynn Conway, associate dean of the college of engineering at the University of Michigan, Ann Arbor, it is hard to imagine coordinating university researchers without e-mail, because their varied class, research, and travel schedules makes them especially hard to track down.

ENGINEERING TOOL. Electronic mail entered the engineering workplace in the late 1960s, when corporate engineering research organizations began communicating with each other and universities over the Arpanet. By the mid-1970s, it was already being viewed by engineers as a powerful tool.

> There is no inertia in the system anymore, and there are times when inertia is a good thing

At the Xerox Palo Alto Research Center (PARC) in the 1970s, collaboration by means of electronic mail allowed then PARC researcher Conway and California Institute of Technology professor Carver Mead to develop their ground-breaking methodology for structured very large-scale integration (VLSI) design. At first they exchanged only text messages between Palo Alto and Pasadena, but soon they were shipping actual instructions for IC layouts electronically over Xerox Corp.'s companywide mail system.

By tapping into the Arpanet, students across the nation could submit design files to an automated file server at PARC. The server would extract chip designs from the e-mail messages, collect designs into manufacturable groups, and convert the data into the appropriate format for semiconductor mask-making.

E-mail is particularly important in making crash projects successful, Conway told *Spectrum*. "It is a powerful medium for small group coordination round the clock," she said. "Because the VLSI design project was intense, e-mail was suitable."

E-mail was also used at Xerox PARC in the late 1970s and early 1980s for the development of Interpress, a printing protocol that has evolved into today's PostScript language. John Warnock, an Interpress designer and now chairman and chief executive officer of Adobe Systems Inc., Mountain View, Calif., has recalled that Interpress designers were scattered among Palo Alto and El Segundo in California and Pittsburgh and Philadelphia in Pennsylvania.

In the early 1980s, Common Lisp, a computer language for artificial intelligence, was designed by a group of some 60 people at numerous organizations collaborating over the Arpanet. The group met just twice in three years, and has indicated that the language development would not have been possible without the Arpanet's e-mail capability.

DOWN SIDE. Electronic mail has its limitations, nonetheless. According to Walker of the DEC Cambridge Research Laboratory, "It is very hard to reach a decision about something that is complex and multifaceted." Walker told *Spectrum* that she has participated in a number of lengthy and deep technical discussions carried on by means of e-mail, but has found that, in the absence of a structured, face-to-face meeting, a participant rarely takes charge, summarizes the data presented, and guides the group toward a solution. "It is great for collecting information, but it is tough to reach closure, because people just haven't worked out the processes yet," she said.

Sociologist Hiltz noted a similar phenomenon in her study of scientists—that half the users felt that theoretical controversies in their fields were clarified by the use of electronic communication, but none felt it helped resolve them.

Engineers who spend too much time reading e-mail lose sight of the forest for the trees, Conway has noticed. "Your point of view becomes skewed to the present, and you lose the ability to manage subtle things that take time to build and grow," she said.

"There is no inertia in the system anymore," said Robert H. Anderson, senior information scientist at the Rand Corp., Santa Monica, Calif., "and there

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tually impossible to figure out," said Larry Landweber, vice president of the Internet Society. Institutions share costs by renting capacity, unlike on Milnet, where users are charged according to the number of packets sent.

In the United States, Government-funded backbones such as NSFnet are ostensibly used for educational and research purposes only. There are also commercial backbones on the Internet, which can sell software or services and offer games with the meter running.

CALLING FIDONET. Unlike the Internet, FidoNet is a telephone-based relay network, requiring people to make calls using existing public phone lines, ideally at regular intervals, to forward e-mail. FidoNet is acknowledged to be in more than 60 countries, including the United States.

Since it does not require much infrastructure, it is easily installed and is therefore common in developing countries, noted Landweber, a professor of computer sciences and a specialist in international networking at the University of Wisconsin in Madison. Because the FidoNet is financed almost entirely by individuals, reducing modem-telephone time has been the priority of the protocols, which now use Zmodem-based transports.

Since November 1991, an experimental system that uses Internet to exchange mail and news between Europe and North America has saved FidoNet operators thousands of dollars a month, according to Randy Bush, Pacific Systems Group, Portland, Ore. FidoNet has tens of thousands of public and private nodes and more than a million users, Bush estimated. The daily volume of compressed electronic news on FidoNet is about 5 Mb.

Another problem with e-mail is the maze of address names. Some business cards display three or more e-mail addresses. An Internet address might look like: jadam@ieee.org; but to pass to FidoNet from the Internet, the address might be: john.adam@p0.f42.n105.z1.fidonet.org. Still other e-mail addresses use ! or % symbols and are even longer.

In contrast, the labyrinth of protocols causes no big hassles for electronic mail. It is relatively easy at a gateway between networks to translate the header from one recognized mail application protocol to another (such as the Open System Interconnection's X.400 to that used on the Internet, SMPT and RFC822).

"We will always see multiple standards out there," said Cerf, because of the installed base, different priorities, and new technology. Even proprietary protocols such as Appletalk and Decnet may be encapsulated and sent across the Internet.

The long-awaited privacy-enhanced electronic mail is just becoming available to Internet users. As companies use networks to send proprietary information, privacy and authenticity become essential. But U.S. export restrictions on certain cryptography techniques may create special islands of users.

Cerf also acknowledged that the system is not friendly to neophytes but rather "is designed and used by people who are comfortable in the arcane world of software." However, this culture is changing, he noted. The growing number of commmercial users will surely not put up with difficult user interfaces and, just as important, will spend a lot of money to spur the market for easy-to-use systems.

—*J.A.A.*

are times when inertia is ■ good thing.''

For those who are new to electronic mail or who use it seldom, the lack of nuance in keyboarded comments poses hazards. Write Anderson and Norman Z. Shapiro in a Rand report: ''Perhaps the most important phenomenon in electronic mail systems is the likelihood that the recipient will react negatively or inappropriately in reading material that might well have been misinterpreted.''

An informal system of ''inflecting'' e-mail, called ''smilies'' has developed, but it does not always register with the recipient. In an electronic mail debate on the risks of the computer revolution, published in the *Wall Street Journal* on April 6, Mitchell Kapor, founder and former chief executive of Lotus Development Corp., Cambridge, Mass., commented: ''Risks, what risks? Computers are here to benefit all personkind.:-)''

But debate participants who did not notice the smilie :-) got into a heated debate over his remark. It was interrupted only when Kapor revisited the conversation three days later and said, ''The typographic glyph :-) which I included at the end of my comment is the on-line equivalent of an ironic or sarcastic tone of voice. It is intended to convey that the writer really means the opposite of the literal meaning of what preceded. . .What I was saying was that there are risks in computers.''

Even when understood, smilies do not eliminate another hazard of e-mail communication—the temptation to ''flame.'' With e-mail it is all too easy to dash off an angry and ill-considered reply to ■ message—much easier than when responding orally or in a formal letter.

Some electronic users are not aware or forget that ''private'' e-mail is not really private; a record of the messages exists on a file server somewhere, is sometimes archived onto tape and stored for years, and can be retrieved by others in ■ company (Federal law prohibits outsiders from snooping into electronic communications, but employers can tap in at will. Other legal protection surrounding e-mail are hazy and are currently the subject of much debate.)

The good news is that important mail accidentally ''deleted'' can be retrieved. The bad news is private mail may be misused; people have been fired because of the content of supposedly private messages. In Colorado City, city council members discovered to their dismay that the mayor was able to thwart them on certain issues because he had been regularly reading their ''private'' communications. And the reappearance of e-mail memos sent and apparently deleted by White House officials was key evidence in the Iran Contra hearings. [Security concerns of computer communications were addressed in the August issue of *Spectrum*, ''Data Security,'' pp. 18–34.]

For its first decades, only a relatively small research community had access to electronic mail. But in the past five years or so, it has become widespread in the biggest corporations, and it will be some more years before it reaches a more general audience. As ■ result, much electronic mail to date has been of some value to the recipient. Nonetheless junk mail has begun to proliferate, and may threaten e-mail's usefulness. To combat the threat, several electronic-mail systems have introduced ''filters'' in various versions.

Some filters sort mail into topic folders defined by the user, so that less important mail may be collected and handled at leisure. Others act as ''bozo'' filters, eliminating messages from certain sources, giving those from key sources high priority, or forwarding some to other recipients for handling. Another type filters out any message sent to more than, say, 20 people, rationalizing that messages with broad distributions either are of little account or will be heard through other means.

Filters, however, are not popular. They prevent people from getting the unexpected message—the new contact, the new information—that is sometimes the most important by-product of electronic mail.

Even nonjunk mail is sometimes overwhelming—25 messages a day can be reviewed and handled in 20 minutes, perhaps, but the several hundreds of messages waiting after ■ two-week vacation are daunting, keeping some engineers and managers from ever really taking ■ break; they check their electronic mail daily, no matter where they are or what they are doing.

A solution suggested by sociologist Hiltz in her 1985 book *Online Communities*—but apparently not widely implemented—is a self-destruct capability: senders can tag messages with the last date of their usefulness, after which they erase themselves. For example, Zmail, ■ mail system used on Symbolics computers, asks for an expiration date in the header of a message, and users choose whether or not to have expired messages automatically deleted.

> Electronic mail cuts across corporations and the hierarchy of organizations, creating a new kind of accessibility

RESTRUCTURING THE ORGANIZATION. By its very nature, electronic mail blasts aside typical corporate hierarchies because the messages are undifferentiated—there is no fancy letterhead or secretary to place ■ call and ask the person called to hold for president so-and-so. In an electronic list of messages, ■ message from a summer intern looks just as important as one from the company president.

Electronic mail, said Lucky at AT&T Bell Laboratories, ''has produced a new social fabric for the R&D community that cuts across corporations and the hierarchy of organizations, creating a new kind of accessibility. It is easier to send e-mail to very important people, people whom you would never consider writing or calling.''

At Tandem, anybody can, and many do, send messages to president Treybig, an open access policy the company believes is one reason for its success.

Electronic mail also eliminates cues about age, gender, race, and appearance: people are judged only by the value of their ideas, so all ideas can get an equal hearing. Carnegie Mellon researcher Kiesler writes: ''When communication lacks dynamic personal information, people focus their attention on the message rather than on each other.''

This may lead to better decision-making. Kiesler and Sproull, also at Carnegie Mellon, concluded in their studies that the best solution may not arise from face-to-face group discussions if it is suggested by ■ low-status person; electronic meetings may find better answers.

And for engineers, Lucky said, e-mail may be ■ better medium for communication than voice. ''I'm shy about talking to people on the telephone that I haven't met in person,'' Lucky told *Spectrum*. ''I would rather deal with ■ computer. It's easier to think with my fingers, and I don't get tongue-tied.''

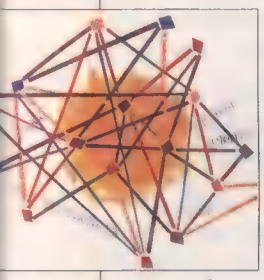
Electronic mail reduces the tendency of the more outspoken personalities to dominate discussions, and therefore allows more diverse ideas to emerge. As Kiesler and Sproull put it, research laboratories have leapers, who think quickly on their feet and love debate, and plodders, who like to work through implications of ideas in detail before sharing their analysis. With electronic mail, both types of scientists get their ideas heard; without it, the leapers dominate.

The ability to communicate across the hierarchy, broadcast to peers in various places in an organization, and form *ad hoc* communities to solve problems will reduce the need for middle management and make corporations more efficient, said Rand Corp.'s Anderson. ''Corporations can be run with thousands of employees less than before,'' he told *Spectrum*, ''and we are already seeing some layoffs result.''

The effect is positive, Anderson indicated, because the talents of individual employees will be able to develop more fully than if they were locked in a traditional physically co-located work group. ''A lot of people will have to find new employment,'' he said, ''but somebody always gets hurt in revolutions, and this is ■ revolution.'' ◆

Playing on the net

Role-playing fantasies and free software await surfers on the nets, who can even compose their own daily 'magazines'



Be it romance or Ren and Stimpy cartoon news, the latest sport scores or movie reviews, developments in politics or computer graphics, many electronic networks are likely to have it—perhaps even more than is good for you.

"I try to stay away from netnews because it can take up so much time," said Larry H. Landweber, a computer scientist at the University of Wisconsin in Madison. But aside from news and discussions, the net can be used to pluck free reports and software. Robert Lucky of AT&T Bell Laboratories, Murray Hill, N.J., for one, likes to cruise recesses of the Internet, downloading electronic music.

First, it is helpful to learn some of the "netiquette" and lingo. Being concise and inoffensive is usually encouraged. Humor is emphasized with a winking smiley face ;-) or laugh :-D. E-mail argot includes IMHO (In my humble opinion) and ROFL (Rolling on the floor laughing).

Many friendships and even marriages have been formed by electronic pen pals. "It's a very safe way to communicate, it draws women in." said Rob Fulop, president of Interactive Productions Inc., Foster City, Calif., who is a peruser of nets.

DIGITAL DATING. A typical dating sequence often involves a hierarchy of communications technologies, as pointed out by "sookie" who herself has "gotten into hot and heavy e-mail." First, it may start with witty digital ripostes in public, she said, followed by individual "long, sensitive e-mail, then photo faxes, then long phone calls." Finally, of course, they may actually decide to "interface" in person.

Whether terminal love or digital dating results in more stable relationships will no doubt be subject to study—people in cyberspace are judged not by looks, accent, or age, but by brains and interests.

Perhaps no country is as wired as France. It has fallen for Minitel, a service supported by France Telecom in Paris, which is now carried by more than 30 percent of the country's phone lines. Some 18 000 services are offered from the small terminals. Besides stock quotes, legal advice, sports, and weather information, Minitel offers tarot card readers, hypnotists, sexologists, travel agents, and dream analysts. Most of the publicity about this net comes from the *messagerie-roses*, which includes singles bulletin boards and soft-porn dialog services. Electronic directories—some very similar to the white and yellow pages in U.S. phone books—are actually the most widely used. Jean-Pierre Casara, president of Minitel Services Co., New York City, said his network is now being offered in the United States as well as other countries.

Many networks have "chat" features, like the Internet Relay Chat (IRC) on that meganet, which allows a user to participate or drop in on real-time talks around the world, switching channels at whimsy. Several networks offer the same smorgasbord of services as Minitel with different twists. The San Francisco–based Well (Whole Earth 'Lectronic Link), for instance, has collaborative poetry compositions [To probe further, p. 33].

While electronic anonymity often fosters openness, a guide to Usenet reminds users that your boss, your friend's boss, and your girl friend's brother's best friend might be scanning your entries: "Think twice before you post personal information about yourself or others. This applies especially strongly to groups like soc.singles and alt.sex. . . . Information posted on the net can come back to haunt you." There are thousands of ongoing discussions or conferences on any topic imaginable. Usenet, created in 1980 by students at the University of North Carolina in Chapel Hill and Duke University in Durham, N.C., is a popular mix of some 3000 sessions that are accessible from many networks and bulletin boards over the world. If a topic is missing, users may easily set up their own sessions.

Also available are text-based fantasy games called MUDs (for Multiuser Dungeons and Dragons), which are accessible on the Internet by the Telnet command. And users can play electronic poker or other games over the net almost as easily as they could in a video arcade.

Often, of course, users combine chatting with tips on hot programs to download. "There's a file [on line, 85 773 bytes called WASHDC23.ZIP] that contains DC area scenery for use with Flight Simulator. Tried and tried to use it with mucho frustration. Then I got the Flight Simulator Aircraft and Scenery Designer, installed it, and now—with a bit of tweaking—I can go zipping around the Beltway, out to Manassas, etc.," wrote one user of a Washington, D.C., area bulletin board system.

PERSONAL MAGAZINES. The best deal, of course, is the public domain software and shareware offered. Usenet has a special 'gnu' tagline for a group from the Free Software Foundation. Any variety of software programs and fixes can be downloaded. Included are games like SFLY11 where flies that invade the user's home must be swatted and, on the darker side, viruses that cause letters to drip from the screen.

Usenet can function like a personalized magazine. Important news announcements, screened by a moderator, may be posted or broadcast to all Usenet users. Individuals also indicate which special interest groups they want to join and are automatically added to the mailing list. So in checking one's daily personal e-mail, it might read like this:

Unread news in rec.humor.funny5 articles
Unread news in comp.graphics 10 articles
Unread news in rec.music.synth 2 articles
Unread news in sci.nanotech 1 article

Users may then check the "headlines" before seeing what articles they want to actually read and, of course, may drop or add groups at any time.

Digital text offers some advantages over its fixed-type cousin. One is that encryption can mask a "spoiler" —such as giving away the plot of a movie in a review. (In Usenet the command "rot13" shifts each letter 13 characters so an "a" becomes an "n.") Similarly, humor having messages offensive to some groups often is encrypted with a warning.

Perhaps the biggest problem is navigating: finding discussion groups and bulletin boards that fit the user's interests and personality. Several projects like the Wide Area Information Servers (by Thinking Machines, in collaboration with Apple Computer, Dow Jones, and KPMG Peat Marwick) are helping to simplify wending through the offerings on the net by simplifying commands.

The good thing about the nets is that there are few editors like those at newspapers who filter material. That is also their weakness. Fortunately, scanning is faster. But as the night wears on, long spells of dross may become irritating and could quash any net addiction—at least until tomorrow. ◆

John A. Adam Senior Associate Editor

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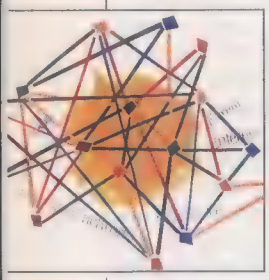
Forces for social change

The international web woven by electronic networks helps empower people around the globe and democratize governments



Gorbachev is sick, perpetrators of the 1991 coup in the then-Soviet Union told its populace via television, radio, and newspaper. The international community supports the new regime, they said.

But within hours computers and facsimile machines from Moscow to Vladivostok were humming with information from around the world that quickly debunked that official story. And in the Russian White House, Boris Yeltsin and his supporters, surrounded by tanks that threatened to overrun them at any time, were reassured by messages received on a Moscow computer that the North Atlantic Treaty Organization (NATO), the U.S. government, and other nations were on their side.

"Those gray men who perpetrated the coup had no conception of what e-mail is," *IEEE Spectrum* was told by Gloria Duffy, president of Global Outlook, an institute in Palo Alto, Calif., that provides research and public education on international peace and security. "It was distressingly easy for them to take hold of the broadcasting and print media outlets and squelch information coming through them, but e-mail broke through the wall of propaganda immediately."

From Tiananmen Square to the Persian Gulf, from Paris to Santa Monica, Calif., electronic mail coupled with fax technology is influencing the outcome of political events.

ELECTRONIC GLASNOST. E-mail routes into the Soviet Union have existed for only a few years. The first was established in 1986, the San Francisco/Moscow Teleport—now Sovam Teleport USA in San Francisco.

In 1990, when the U.S. government permitted links between Internet, a government-subsidized research network, and Soviet networks, Sovam Teleport was quick to establish one. (Electronic mail users in the former Soviet Union had previously been able to send e-mail to Internet by calling a computer in Finland, which could make phone connections to the USSR with relative ease. Soviet residents have also been able to reach networks like CompuServe through Finland and other countries.)

In the late 1980s, a private company in Moscow, Demos, set up a network called Relcom, now in 70 Soviet cities. A widely accessible commercial network, Relcom also communicates with the Internet (Demos has since separated from Relcom).

Just five months before the coup, in March 1991, yet another network, this one nonprofit, was established in the then Soviet Union. GlasNet, a joint venture between the Institute for Global Communications, San Francisco, and the International Foundation, Washington, D.C., is accessible from most of the new Commonwealth of Independent States (CIS). It is linked to a number of international politically progressive networks, including the British-based GreenNet, the U.S.-based PeaceNet and EcoNet, and the Brazil-based AlterNex.

And throughout the former Soviet Union, in the last few years, individuals have begun operating direct-dial electronic bulletin boards from their homes. These bulletin boards also exchange information in a loose network (where independent operators send messages on an informal basis).

New links to the international nets are appearing every year. Approaching Russia from the east, the University of Alaska in Fairbanks established in August a direct communication link with the Russian Far East city of Magadan to provide telephone and e-mail service to three institutes of the Russian Academy of Sciences.

So unbeknownst, apparently, to the conspirators when they made their 1991 grab at control, an electronic spider web was lying in wait to thwart them.

Wrote Robert B. Reich in the *New Republic* in 1987: "Many of the new technologies are themselves subversive. Computers... and telecommunications equipment not only incite unorthodox ideas, they also allow them to be exchanged instantly. They inspire communities of dissent."

Said Shel Hall, who moderates political discussions on CompuServe: "I suppose this means that during the next coup the authorities will be wielding wirecutters as well as bayonets." But had the coup perpetrators been aware of the power of electronic communications, they might still have found those links impossible to break.

In case soldiers marched in and seized the main network computers (an event that never occurred), Relcom and GlasNet planned alternative ways of staying in touch with the networks, no matter what.

"Most e-mail operations can be done with a laptop," Geoff Sears, executive director of the Institute for Global Communications, told *Spectrum*. "So they couldn't have stopped it without shutting down their entire phone system," which they needed for their own purposes.

Among the messages that came across the networks during the coup were those exchanged with Nikolai Kapranov, a defense advisor to Boris Yeltsin. He was communicating from Moscow—possibly from one of the computers inside the Russian Parliament, then surrounded by tanks. Kapranov, through PeaceNet, sent detailed accounts of the events at Parliament as they occurred, urging recipients to forward them to the U.S. media. At Global Outlook, which had been working with Kapranov on a project, a news reporter watched the messages as they arrived.

In return, Global Outlook staffers prepared long texts summarizing responses by the U.S. and other governments. Kapranov printed and distributed this news to the people holding off the tanks. It was also used as source material for an independent radio station that was broadcasting out of the Russian White House.

NATO officials bolstered Yeltsin's defense with messages of support through the e-mail link to Kapranov.

"[Kapranov] told us later this information had been very encouraging for people," said Global Outlook's Duffy. "The coup perpetrators had been publishing information that said the outside world supported them and it was all over for Gorbachev. The information from us said the opposite."

After the coup was defeated, Kapranov sent this message to NATO headquarters and Global Outlook: "Dear everybody, Thank you for your support, information you provided after being translated, was spreaded as leaflets and defenders of Russian Parliament, was on the Radio Station of Russian Parliament, the only Radio in Moscow that provided those times with correct information, it was also spreaded among militaries. It was also important for people inside Parliament building to know that they have connection with Democratical countries and to feel their support. Again thank you."

Tekla S. Perry Senior Editor

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Glasnet also played an important role in exchanging messages between cities in the Soviet Union about organizing local resistance and spreading Yeltsin's proclamations around the country. Relcom, too, was used by resistance organizers in the remote reaches of the Soviet Union to plan demonstrations and obtain news updates that were printed and posted publicly.

All this communication, said Don Reich, manager of customer relations for Sovam Teleport, "gave people the security of knowing that even when a country's political system gets shaky, they were guaranteed a connection to the outside world."

> 'Networks have the effect of letting things get out and bringing in all sorts of new information and ideas'

TIANANMEN SQUARE. Only a few strands of the electronic communications web were in place in 1989 when the students in China revolted, making their stand at Tiananmen Square.

"The failure of Tiananmen Square was a failure of the distribution of data," said John Gage, director of the science office for Sun Microsystems Inc., Mountain View, Calif. Because of inadequate telephone connections outside of Beijing, e-mail was useless in spreading the information that could have strengthened resistance.

As a matter of policy, the government of the People's Republic of China (PRC) had limited electronic communications to the outside world to reduce information flow, which they recognized as dangerous to their regime, Gage told us. Currently, a small number of circuitous routes to China through Europe do exist. The Chinese Government officially forbids transnational data flow.

What the PRC Government had not limited, however, was the fax. China tried to resist the use of fax machines, said Marshall Strauss, executive director of the Democracy for China Fund, Newton, Mass. But they have become vital for conducting business with the outside world and therefore are key to the Chinese economy. So the resistance was able to exploit fax technology, particularly for distributing objective reports of events in China and of the outside world's reaction to resistors within Beijing. "Chinese students were aware of the importance of the international community and wanted to stay in close contact," Strauss said.

During the Tiananmen uprising, expatriate Chinese would send faxes to any fax number they knew in the PRC, rotating fax numbers, since regular recipients of forbidden information risked arrest. At friendly faxes, the information was received, stripped of identifiers, and distributed.

"Fax had a lot of power," said Sun Microsystems' Gage. "A copy of a news article, with the *New York Times* banner, has more éclat" than a text message or a transcribed telephone conversation.

At several U.S. organizations, office space, with computers, fax machines, and phone lines, was made available to Chinese students, who used international electronic mail to organize their activities.

The most dramatic use of fax after the massacre, Strauss said, came toward the end of 1989. That fall, Chinese activists used the international e-mail networks to coordinate an "international fax blizzard" into China, faxing a fake edition of the *People's Daily* from around the world into hundreds of Chinese Government, Communist Party, and other offices associated with the ruling elite.

The Chinese Government, however, though not able to stop the flow of faxed information, was able to inhibit it. Since not many fax machines exist in China, the Government posted guards at the ones it knew about. The revolutionaries were able to fool the guards to some extent by starting faxes with a few pages of innocent material, followed by politically important documents, by which time, said Strauss, "the guards would get bored and go back to their card game." But this policy of guarding fax machines was chilling to dissenters. In some cases, arrests were made, and soldiers did cut some phone lines, reports say.

The exile community continues to use fax and electronic mail to organize against the PRC government. Three years after the uprising, the international web of electronic mail has yet to embrace China, but links are beginning to be established.

China is also working to modernize its telephone system, which will make internal e-mail networks easier to create. Soon, said

AP/Wide World Photos

'. . . Moscow is full of tanks and military machines, I hate them. They try to close all mass media, they shutted up CNN an hour ago, Soviet TV transmits opera and old movies. But, thanks heaven, they don't consider Relcom [e-mail] mass media or they simply forgot about it. Now we transmit information enough to put us in prison for the rest of our life :-) . . . .'

During 1991's attempted coup in the Soviet Union, while tanks surrounded the Russian parliament, resisters used e-mail to communicate with the outside world. This message was relayed over the Internet to the United States.

Gage, "with the advent of global satellite networks, there will be no possibility to control the flow of information."

HOTSPOTS. The worldwide web of e-mail is growing. For example, the Institute for Global Communications (IGC) has helped set up systems in Brazil, Ecuador, and Nicaragua. The governments in each country have been supportive.

"They are enthusiastic because they see us bringing computing resources into a developing country," said IGC's Sears. "They don't totally understand what they are getting into, that networks have the effect of letting things get out and bringing in all sorts of new information and ideas."

The networks may often create unanticipated links. While the U.S. government prohibits phone service to Cuba, and Cuba would rather prevent communications with the United States, anyone on Internet can send e-mail to people in Cuba. (The messages travel through Canada.)

These international networks are being used daily by political groups. Most uses, however, never come to light, since much of e-mail's content is not tracked by network managers.

EcoNet, operated by the Institute for Global Communications, got heavy use during this year's Earth Summit, as nongovernmental organizations found it an easy way to collect information and plan events. Previously, organizers of Redwood Summer, an Earth First-led series of protests against loggers in the Northwest, used EcoNet to debate and plan strategy.

PeaceNet is used by Amnesty International, London, to distribute reports and "Action Alerts," to mobilize volunteers around the world.

In Central and South America, governments at various times have closed down the independent press. When that happens, a network of fax machines goes into play; articles from the United States are sent by fax, quickly photocopied, and distributed on the streets.

In France, the Government-run Minitel is used for political organizing. This network was installed originally to replace phone directories and quickly evolved into a plethora of information services and related activities. But since the late '80s, when students nationwide organized a strike and marches protesting increases in student fees, "every political movement in France regularly uses Minitel," said Jim Warren, a computer rights activist who is on the board of Autodesk Inc., Sausalito, Calif.

During the Persian Gulf War, e-mail acted as an alternative news source. In the Middle East, local networks hummed as people traded war stories and rumors. News also traveled around the world over corporate networks from offices in the Middle East. And much information found its way onto commercial networks.

PeaceNet was used extensively to organize opposition to U.S. involvement in the Gulf. A 20-page background paper sent into the net by a national Quaker group was printed at numerous points in the United States and distributed widely. Protests were organized, and Congress was snowed under with fax messages. "Usage of our system quadrupled," Sears told *Spectrum*. "The load was so heavy it almost shut us down." PeaceNet became so recognized as a protest tool that local police departments began logging on to get advance notice of peace demonstrations.

U.S. ACTION. This year, the United States is beginning to see e-mail used in national political campaigns. But, said Matisse Enzer, head of customer support for the Whole Earth 'Lectronic Link (Well), a computer conferencing and mail system based in Sausalito, Calif., "this is one election too soon" for e-mail to have a real impact. Most established political organizations have yet to look at its potential.

Democratic contender Jerry Brown went the furthest, establishing addresses on the Well, PeaceNet, and CompuServe. Brown even spent 2 hours live on CompuServe, responding to questions. "This was one of the first times a national presidential candidate has come on-line to carry on a dialog with the public," said Autodesk's Warren.

> 'We live in virtual space'

Warren has been trying to organize an e-mail presidential debate that would be carried on Usenet, a sort of electronic newspaper that reaches more than a million people through Internet and FidoNet. Early on, Brown, Arkansas Governor Bill Clinton, and libertarian candidate Andre Marrou committed to the debate. President Bush has not responded. If the '92 debate does not occur, Warren said he will try again in '96. The Bush and Clinton campaigns are currently posting statements and fielding voter questions on the Prodigy network.

On a local political scale, the nets are having a bigger impact. One example of a community that uses electronic mail and bulletin boards extensively to give citizens better access to government is Santa Monica, Calif. In 1989 the city installed an electronic communications system free to any resident. Called the Public Electronic Network (PEN), it offers, in addition to electronic mail, databases about city council activities, the public library catalog, and computer conferences on a host of topics (rent control is a hot issue). Questions e-mailed to city officials (over 200 monthly) are answered within 24 hours.

Some 5000 residents use the system regularly. A group that organized electronically over PEN recently persuaded the city council to allocate US $150 000 to funding showers, lockers, and laundry facilities for the homeless. Another electronically organized group has blocked the development of a city-owned beach estate into a luxury hotel.

While a number of U.S. political groups are currently looking into ways they might use e-mail to facilitate their activities, e-mail is the lifeblood of one organization: Computer Professionals for Social Responsibility.

"We live in virtual space," Mark Rotenberg, director of the group's Washington, D.C., office, told *Spectrum*. The national organization supports socially beneficial uses of technology; its 2500 members communicate through the Internet.

POTENTIAL HAZARDS. Widespread use of e-mail for political purposes is not without hazards. It would be easy, for instance, for someone to change the text of a message from a presidential candidate, Sun's Gage told *Spectrum*. This could have international implications.

And impersonation is easy: someone on CompuServe this spring presented himself as an official representative of Ross Perot until the Perot campaign shut him down. The impersonator was a Perot fan, and did it out of misplaced enthusiasm rather than mischief.

But access would have been just as easy for a less benevolent impersonator. A number of years ago a network prankster reportedly sent messages that appeared to originate at "kremvax" (Kremlin VAX computer) in the Soviet Union, sparking concern from U.S. military officials.

It is also easy to use networks for propaganda. Currently, said Larry Landweber, professor of computer science at the University of Wisconsin in Madison: "There is a lot of propaganda flowing now about Croatia and Serbia; it is hard to tell where it is generated."

Networks can even be used for terrorism. "What if on Internet hundreds of thousands of people who were disgruntled with Washington sent messages among themselves, agreeing that at noon on such and such a day, they would all call any number in the 202 area code simultaneously?" asked Robert H. Anderson, senior information scientist at the Rand Corp., Santa Monica, Calif. "That would shut down the D.C. phone system for hours."

Enzer at the Well said such a scenerio is unlikely. "It is easier to be creative on this medium than to be destructive," he noted. "Getting large numbers of people to do something via the Internet is like herding cats."

Despite these risks, few are questioning the power of the networks for global good. International networks, said Sears at the Institute for Global Communications, "are the only way to approach solutions to problems that defy national efforts, like global warming, ozone degradation, and pollution of the oceans."

The networks also, Sears said, "just by helping people have greater contact with people of other nations and alternative sources of information about them," are a force for world peace. ◆

To probe further

Connections: New Ways of Working in the Networked Organization, by Lee Sproull and Sara Kiesler (MIT Press, Cambridge, Mass., May 1991), analyzes e-mail and includes case studies of several high-technology firms. The paperback is to be out this month. *Online Communities: A Case Study of the Office of the Future*, by Starr Roxanne Hiltz (Ablex Publishing Corp., Norwood, N.J., 1985), and *Computerization and Controversy: Value Conflicts and Social Choices*, edited by Charles Dunlop and Rob Kling (Academic Press, San Diego, Calif., 1991), are useful, too.

Also worth reviewing are *The Matrix: Computer Networks and Conferencing Systems Worldwide*, by John S. Quarterman (Digital Press, Bedford, Mass., 1989), and "Towards an Ethics and Etiquette for Electronic Mail," a report by Norman Z. Shapiro and Robert H. Anderson (Rand Corp., Santa Monica, Calif., July 1985).

Then the August 1992 issue of *Network Computing* features a special report: "E-mail Applications: the New Building Blocks of Business." *Whole Earth Review* (27 Gate Five Rd., Sausalito, Calif. 94965) published several articles on "Electronic Democracy" in its Summer 1991 issue. And *Boardwatch Magazine*, Littleton, Colo., is a monthly with information on bulletin boards and on-line services, including classified advertisements of all sorts of bulletin boards accessible by modem; 303-973-6038.

"Inside the PARC: the 'information architects,' " *IEEE Spectrum*, October 1985, pp. 62–75, shows the early use of e-mail inside Xerox Corp.'s Palo Alto Research Center (PARC). Network security concerns, including some e-mail ruses, were addressed most recently in *Spectrum*'s special report, "Data Security," August 1992, pp. 18–45.

How networks helped debunk cold fusion claims of 1989 is portrayed in *Too Hot to Handle: The Race for Cold Fusion*, by Frank Close (Princeton University Press, Princeton, N.J., 1991). Seymour E. Goodman wrote on "Political Activity and International Computer Networks" in the February 1992 *Communications of the ACM*, p. 174.

The Computer Professionals for Social Responsibility will hold their annual meeting on Oct. 17–18. Contact Nikki Draper at 415-322-3778 (cpsr@csli.stanford.edu) for more information.

For the proceedings of INET '92, the annual conference of the Internet Society, write to Publications Office, Internet Society, 1895 Preston White Dr., Reston, Va. 22091.

Founded in 1983, the Electronic Mail Association (EMA), Arlington, Va., is a nonprofit trade group representing 350 user and vendor companies. A February 1992 publication, "Electronic Mail Market Research Results," studies e-mail users in Fortune 2000 and equivalent corporations in North America. The cost is $45 for nonmembers.

Also available to nonmembers are "EMA Update and Focus on Applications," "A User's Guide to the Electronic Communications Privacy Act," "Access to and Use and Disclosure of Electronic Mail on Company Computer Systems: A Tool Kit for Formulating Your Company's Policy," and "The Electronic Mail Advantage: Applications and Benefits." Contact: Electronic Mail Association, 1555 Wilson Blvd., Suite 300, Arlington, Va. 22209-2405; 703-875-8620; fax, 703-522-0241.

A useful reference guide is the *1992 Information Industry Directory*, 12th edition, edited by Bradley T. Morgan (Gale Research Inc., Detroit, Mich., 1992). It provides a list of organizations whose information systems and services include capabilities that allow clients to electronically send and receive messages. ◆

Selected on-line services

Many options, too numerous to list entirely, are available to those interested in getting on electronic networks. The IEEE itself is linking all its global sections by using the Internet and other networks. More details will be published later in THE INSTITUTE. Those already linked electronically to the Internet can request a guide by sending a message to "email.guide@ieee.org."

There are also a number of services that allow users to connect to various U.S. bulletin board systems with a local telephone call. Intellibusiness, a service offered by Bell Atlantic, is one example; 800-543-8843.

Some of the larger network services include:

CompuServe: a smorgasbord on-line service, based in Columbus, Ohio, that is renowned for its technical support. Almost every large personal computer maker and software developer is on this net to respond to user questions. Basic costs are US $49.95 for start-up software and $7.95 per month for basic services, plus a $12.80 hourly rate for extended services; 800-848-8199.

Delphi: a relaxed national bulletin board system based in Cambridge, Mass. There are several commercial plans. The basic "10/4 plan" costs $10 per month for 4 hours' usage; 800-695-4005.

Echo: the "East Coast Hang Out" service that is the New York City-based equivalent of San Francisco's Well national bulletin board system. Cost is $18.95 per month for 30 hours, $12.95 for students and senior citizens; 212-255-3839.

GEnie: a service offered by a Rockville, Md., subsidiary of General Electric Information Service that has the broadest business and financial information and allows bond and stock trading. Registration is free; basic costs are $4.95 per month and $18 per hour during prime-time hours (8 a.m.–6 p.m., Mon.–Fri.); all other times, no charge for basic services; value services, $6 per hour; 800-638-9636.

Internet: an international net that allows users to share information globally. Those unable to get on Internet through a regional network should contact the NSF Network Service Center, run by Bolt, Beranek and Newman Inc., Cambridge, Mass., by sending e-mail to nnsc@nnsc.nsf.net. The center also publishes a newsletter and an Internet Resource Guide. It is available electronically for free or for $25 for a hard copy; 617-873-3400. Many other Internet guides are available on networks. For example, SRI International, Menlo Park, Calif., publishes one for beginners, "Internet: Getting Started," available from nisc@nisc.sri.com for $39; 415-859-3695.

Knowledge Index: a commercial database service of technical and popular articles associated with the more extensive Dialog but cheaper. Use is restricted to nights and weekends. Two sign-up plans are offered: a $30 plan includes 1 hour of new-user credit, while the $40 plan includes 2 hours of new-user credit; the hourly rate is a flat $24. Call 800-334-2564 for information on either Knowledge Index or Dialog.

Minitel: a very popular government-subsidized service in France that is being offered in the United States by Minitel Services Co., New York City. Costs for accessing the French service vary from $0.15 to $1.83 a minute; 212-399-0080.

Peacenet and Econet: services that link activists in the United States with those in other countries. They charge a $15 registration fee, plus $10 a month (including one hour of use) and $10 per hour peak time (7 a.m.–6 p.m., Mon.–Sun.); off-peak, $5 per hour; 415-442-0220; fax, 415-546-1794.

Prodigy: a venture of Sears, Roebuck & Co. and IBM Corp., based in White Plains, N.Y., that is the easiest U.S.-based service to use and has attracted more than 1 million subscribers. It carries many advertisements and has limited e-mail capability, but it plans to join other commercial networks and link to the Internet. There is no hourly fee. Costs are $50 for start-up software and $13 per month; 800-284-5933.

The Well: the Whole Earth 'Lectronic Link, based in Sausalito, Calif., that costs $15 per month plus $2 per hour; 415-332-4335; modem, 415-332-6106.

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Memory catches up

While main memory systems—the domain of the dynamic RAM—grew in size and density, processor speeds raced ahead

In the last decade, the design priorities for microprocessors and main-memory chips diverged. While microprocessors became much faster, memory chips grew in density and size. Now the divergence has grown so great that a fundamental change in memory architecture is required if memory is not to be a drag on computer systems.

That is not to call cramming more storage elements onto a silicon die an unnecessary or trivial development. The consumer demand for performance was after all causing processors to double and quadruple their addressing capability from 8 to 16 to 32 bits. Without an increase in bit densities, therefore, main memory systems would have mushroomed in physical size and cost, while plunging in reliability. At last decade's density, four thousand 16K-by-1-bit dynamic RAM (DRAM) chips would be required for today's typical PC main memory, not the eight 1M-bit chips now usual.

However, while the amount of data that can be stuffed into a square of silicon is not an issue, the gap between memory and processor rates is. Consider the prototype Alpha processor chip recently unveiled by Digital Equipment Corp., Maynard, Mass. [*IEEE Spectrum*, July, pp. 26–31]. It needs to be fed data every 5 ns when working with a 200-MHz clock. But today's fastest standard DRAMs are about an order of magnitude slower. The 4M-bit AAA4M2000 from NMB Semiconductor Co. in Tateyama, Japan, has an access time of 40 ns and a cycle time of 80 ns and is, according to Tom Goodman of NMB's U.S. subsidiary in Chatsworth, Calif., "positioned at or near the practical limit of standard DRAM performance." If processor rates increase by a factor of 10 over the next few years, as Alpha architect Richard Sites and others predict, standard DRAMs just will not work.

Richard Comerford Senior Editor
George F. Watson Senior Editor

Even today, writes Ray Ng of Sun Microsystems Inc., Mountain View, Calif., in "Fast computer memory" [pp. 36–39], resort must be made to ingenious operating modes, such as page mode, and equally ingenious memory architectures, employing caching and interleaving. Only with their aid have computer manufacturers been able to keep slow but inexpensive DRAM chips in their pivotal role as main memory. But the point has been reached where such tricks alone will not make up for the lack of memory speed. Instead, according to Ng, new DRAM-based chip designs will be called upon to cope with what computer manufacturers have in store.

And the computer's central processor is not alone in demanding higher memory performance. The graphics and communications capabilities that users are pressing for in their systems further aggravate the need for speedier memory, as do the superscalar and parallel processing architectures that are entering the mainstream.

Noncomputer applications are being equally exacting, if not more so. High-definition television (HDTV) is likely to be the largest single application for DRAM in the second half of this decade. Roelof Salters of Philips Research Laboratories in Eindhoven, the Netherlands, in "Fast DRAMs for sharper TV" [pp. 40–42], argues that HDTV will require even greater memory throughput than computers do, so needy are future television features such as high-definition display and picture enhancement.

> Standard dynamic RAMS are now at or near the practical limits of their performance

Memory chip manufacturers have not been oblivious to what has been happening in their customers' end markets. The set of articles titled "A new era of fast DRAMs" [pp. 43–49] describes three of the most recent examples of memory architectures for boosting speed—cache DRAM, extended DRAM, and synchronous DRAM—and explores their operating characteristics. The first two of those architectures are now available from their respective originators, Mitsubishi Electric Corp., Tokyo, and Ramtron International Corp., Colorado Springs, Colo. And if those developing a standard for the Joint Electron Device Engineering Council (Jedec) have their wishes for speedy acceptance fulfilled, the synchronous DRAM may be available in sample quantities as this issue arrives at your door. The synchronous DRAM differs from earlier devices in many ways, not the least of which is its open architecture, developed with the participation of leading memory developers.

A fourth dynamic memory type, the Rambus DRAM can be licensed from developer Rambus Inc., Mountain View, Calif. It, too, is now available from several vendors in sample quantities. But unlike the new DRAMs previously mentioned, it does not go out in the world alone. It is accompanied by design specifications for and sample implementations of a memory bus, memory modules, a controller, interface cells, and protocols. Described in "A fast path to one memory" [pp. 50–51] by the company's Mike Farmwald and David Mooring, the fully developed memory system environment is able to transfer data at 500 megabytes per second. Using the Rambus scheme, designers can now easily create compact systems in which a single memory system serves for applications, graphics, audio, and other functions.

Some argue, however, that a bus architecture will not be fast enough to handle the data rates envisioned for the types of applications and features looming on the horizon. A number of professionals with that view have formed the P1596.4 working group within the IEEE Computer Society to develop an open architecture for memory systems, dubbed RamLink. In "A RAM link for high speed" [pp. 52–53], five members of the working group outline a ring architecture for a memory system that performs at very high rates. What's more, it does so even when the use of dynamic RAMs with on-chip caching is not effective—a possible problem with multiprocessor systems.

The final article in the series, "Fast interfaces for DRAMs" [pp. 54–57], deals with a newly developing specialty within the semiconductor industry: the design of high-speed transceiver logic. Because data is moving so swiftly from memory chips to other parts on a printed-circuit board, interface logic and board traces behave as trans-

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mission lines, and effects such as reflection and reactive loading must be taken into account. Separate sections of this article examine center-tap termination, Gunning transceiver logic, and low-voltage differential signaling. ◆

Defining terms

Access time: the time interval between the instant at which data is called for (read operation) or requested to be stored (write operation), and the instant at which it is delivered or completely stored, respectively.

Copy back: see write back.

Cache hit: a request for data that turns out to be resident in cache, so that memory operations can be quickly executed from cache.

Cache miss: a request for data that proves not to be resident in cache, so that the desired data must first be summoned from main memory before an operation can be performed.

Cycle time: the time between the instant memory is accessed and the instant at which it may validly be accessed again.

Dynamic RAM (DRAM): a RAM that uses a single transistor-capacitor pair, or cell, to store each bit of information. It is called dynamic because the capacitor must be recharged periodically ("refreshed") for the information to remain in place.

Fill bandwidth: the rate at which data is transferred from a memory array to on-chip latches or to cache memory, customarily expressed in megabytes per second.

Interleaving: a method of distributing consecutive memory addresses among a number of memory banks so as to increase the rate at which data may be made available to the requester.

Page mode: a means of memory addressing built into a memory chip whereby a block of sequential data can be accessed without certain address information having to be repeated, thereby speeding up data access.

Pipelining: a technique for speeding up processors by dividing the task of executing an instruction into a number of stages and having all stages working on the various tasks concurrently but on consecutive pieces of data.

Read latency: the time between a memory request and the arrival of data.

Static RAM (SRAM): a RAM that uses a flip-flop or latch as a cell to store each bit of information. The cell can adopt one of two states that will remain unchanged, or static, until it is intentionally altered.

Throughput: the amount of data that is handled in a given period of time.

Wait state: an extra processor clock cycle inserted in the execution time when the processor must wait for memory or I/O.

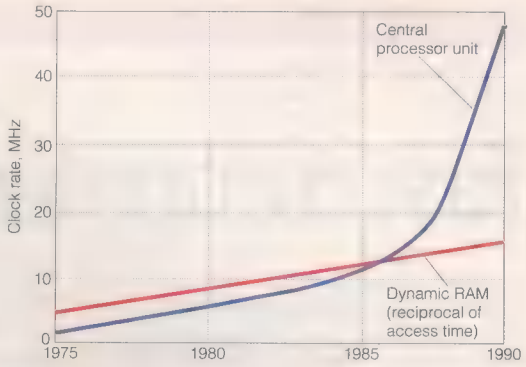
Write back: the writing of data stored in a cache block to main memory before that block is replaced with new data from main memory.

Write latency: the time between a memory write request and the storage of the data.

Write posting: the capture of an address and its associated data to allow a write operation to be performed in parallel with other operations, thus reducing the effects of write latency.

Write through: the writing of data stored in a cache block to main memory while the same cache is being written to.

Until 1985, the clock rates of processors and dynamic RAMs were nicely matched. Since then, processor speeds have soared, while memory speeds have risen only linearly.



Rambus Inc. (photos)

Clean, high-speed transmission of data, like that from a 4.5M-bit Rambus dynamic RAM [left], needs a design focus on interface circuitry, buses, and dense packaging as a whole, as in the Rambus module [below].

Fast computer memories

Designers are searching for new DRAM technologies to reduce memory access time and so unleash computer performance

If the price-to-performance ratio of computer systems is to keep improving, the gap in speed between processors and memory must be closed. Processors perform at their peak only when the flow of instructions and data from memory is fast and unfaltering.

An ever-flowing stream is particularly necessary to reduced-instruction-set computing (RISC) processors, which have become very popular during the last few years. A heavily pipelined RISC processor can execute an instruction every clock cycle, demanding a lot of the memory system. Both superscalar processors, with their multiple functional units, and multiprocessor machines make even greater demands on memory systems.

Nor is the central processing unit (CPU) the only consumer of memory bandwidth. Computers now are expected to be easier to use and more capable than their predecessors, and some of the new capabilities will require speedier memory. Examples include the rapid display of high-resolution graphics in true color, the recognition of speech and handwriting, recording and playing back video and audio, and, ultimately, support of a virtual-reality environment. The machines may also need buffer memory for messages moving over the multigigabit-per-second networks expected in the near future.

These lofty I/O ambitions all involve processing and moving large amounts of data. On top of even faster CPUs, they will strain both memory capacity and memory bandwidth. But the accepted dynamic RAM (DRAM) architectures and solutions have been pushed to their limits. A basic change in architecture seems the only way to obtain an urgently needed increase in memory speed.

The need for change has struck a number of chip makers, because innovative architectures distinguish a variety of recent high-speed DRAMs, which go by such names as synchronous, cached, and Rambus DRAMs. The newcomers may be usefully surveyed from a system perspective, to see how they may solve design problems, particularly with regard to main memory.

Ray Ng Sun Microsystems Inc.

MEMORY LINE. Till now, in the familiar stored-program computer described by von Neumann, the processor has been connected directly to memory (as well as to input/output). From this model, a hierarchical memory system has evolved in which a little, very fast memory is placed very close to the processor and fed by lots of slower memory farther away from the processor [Fig.1]. This hierarchy, which is used in almost all computer systems today, reflects one of computer design's truisms, "fast memory is expensive and slow memory is cheap."

At the first level of the hierarchy are the processor's internal registers. Access to these registers is very fast because they are on the processor chip. However, their number is limited by the available chip area, or "real estate."

At the second level, between the processor and slower main memory, is a cache—a small, very fast memory. The cache is loaded with copies of those blocks of data stored in main memory that the processor is most likely to want for the operation it is currently performing. (Typically, the block size ranges from 16 to 64 bytes.)

> Processors can perform their best only if the supply of instructions and data is fast and unfaltering

If the processor finds the data it wants in the cache (referred to as a cache hit), then to the processor it will look as if main memory is as fast as cache. But if the processor does not find what it needs in cache (a cache miss), then the block containing the missing data must be brought in from main memory, slowing down the system.

Caches usually provide a speedup because they exploit a general characteristic of programs: locality in space and time. Spatial locality indicates that if a location in memory is accessed, then others nearby will probably be accessed soon; temporal locality means that if a location in memory is accessed once, then it will probably be accessed again soon.

One problem with caches is that, in order to be effective, they require very fast RAMs that run at about the same speed as the processor; and while static RAMs (SRAMs) can deliver the required speed, they are expensive. Also, caches must keep track of which memory blocks are in the cache and what their state is, and therefore require a special controller and a tag memory that add complexity and take up precious board real estate. All the same, caches are popular.

It is possible, too, to build systems with more than one level of caching, using on- and off-chip memory. Many modern processors have on-chip caches, for both program instructions and data, that are closer than an external cache and so faster to access. But like the number of registers, the caches have to be small because chip real estate is limited and in many systems they are supplemented with an external cache. The internal cache is referred to as first-level cache and the external as second-level.

The third level of the hierarchy is main memory itself. Main memory is used to store programs and data, and as a source of input and destination for output. Typically, this memory is much larger than cache and is constructed of DRAMs, which are slower than the SRAMs but also less expensive.

The fourth level of the hierarchy is mass storage. Today magnetic-disk storage is ubiquitous. It is used to implement a technique called virtual memory, which fools the processor into thinking the main memory is much larger than is the case. With virtual memory, the processor's address space is divided into blocks of fixed size, called pages. Pages are much larger than cache blocks, usually 4–8K bytes.

Disk bears much the same relationship to main memory as main memory does to cache. Pages are called from disk and placed in main memory when they are needed or returned to disk when they are not. As with cache, the principle of locality is basic. To maintain order in the system, a memory management unit (MMU) keeps track of which pages are in main memory and what

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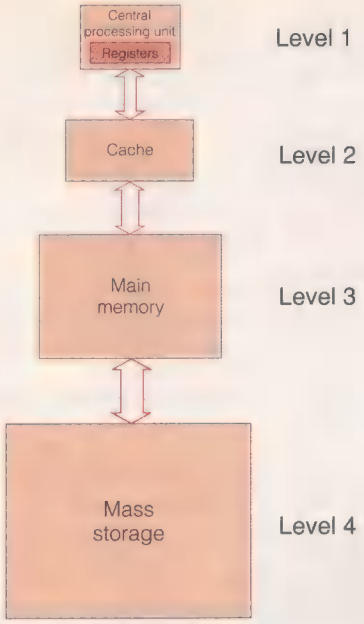


[1] In most computer systems today, the total memory consists of a hierarchy of media. Passing from the top to bottom of the hierarchy, the density of the medium (the amount of data it can store per unit area) increases, while its speed in delivering data and its cost per bit decrease. Some new dynamic RAM (DRAM) technologies aim at simplifying this hierarchy by speeding up main memory to the point where the need for a separate, external cache is moot.

their status is.

As with a cache miss, performance falls off whenever a page is not in main memory when needed (a page fault). The penalty is, however, higher because mechanical disks are much slower than semiconductor main memory. But disks are very cheap, in terms of cost per bit, and can store vast amounts of data; hard disks today commonly store hundreds of megabytes, and the use of magneto-optical and optical discs capable of storing gigabytes is growing.

Strictly speaking, there is a fifth level of storage, for data that will not be used for an extended period of time or whose importance demands its preservation. This archival storage often consists of magnetic tape; of course, removable magnetic and optical discs are also used for long-term storage of programs and data. This storage level has no impact on run-time system operation and so will be ignored for now.

MAIN EVENT. Main memory is almost always implemented using DRAMs, which in both speed and price lag behind the SRAMs generally used for cache. DRAMs use one transistor-capacitor pair, referred to as a cell, to store one bit of information, while SRAMs use a four- or six-transistor flip-flop to store each bit. Because each DRAM cell is very small, DRAMs can be made very dense; the densest DRAM now available is a 16M-bit part, while the densest SRAM is about 4M bits. The per-bit cost of SRAM, depending on its speed, is 5–10 times that of DRAM.

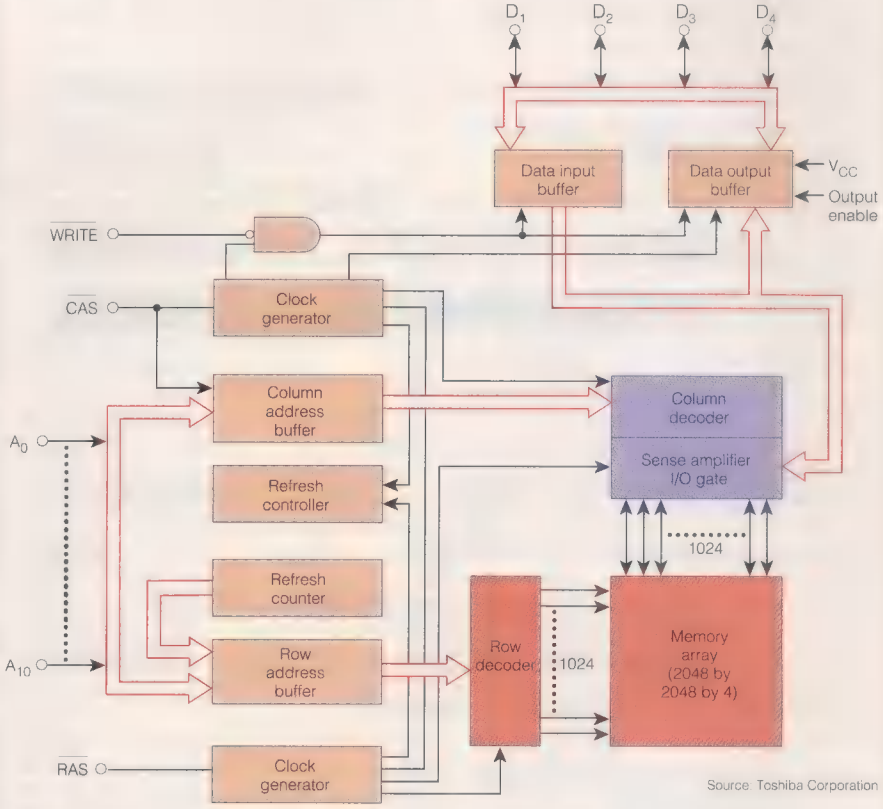
However, because the charge leaks away from the DRAM cell's capacitor, it must be restored by periodic refreshing. Also, the act of reading a DRAM involves transferring and sensing mere dribbles of charge; since each read operation disturbs the cell contents, it, too, requires that the data read be restored. For these reasons, DRAMs are not especially fast.

A DRAM is built as a square or rectangular array of cells [Fig. 2]; to read or write data, the processor sends an address to the DRAM, which typically it multiplexes, supplying first the row address, then the column address. For currently available DRAMs, the time it takes a row address to access a cell is about 40–80 ns, for a column address, about 20–40 ns, and the precharge time is about 30–50 ns. Thus the cycle time (the minimum amount of time between memory accesses by the processor) is about 110–150 ns. In contrast, the cells in small CMOS SRAMs may be accessed every 8 ns; larger SRAMs have a longer access time of about 15 ns.

To raise their operating speed, DRAMs have a special operating mode that takes advantage of their internal row-and-column structure, known as page mode. In this mode, when an entire row (or a chip page, but not to be confused with the virtual memory page) is read into the sense amplifiers, the user can keep the row active and merely change column addresses to access all the data. As long as the accesses remain in the page, the DRAM can work faster. For current DRAMs, the page-mode cycle time (or minimum time between column addresses) is about 40–50 ns [Fig. 3].

SPEEDING UP MAIN MEMORY. A main memory system has three crucial attributes: size, latency, and throughput. Size is affected by density, or the number of bits that can be packed into a given area; the higher the density, the better. Latency is how long it takes for data to be delivered after it has been requested, and is closely related to a DRAM's access time; the shorter the latency, the faster the DRAM. Throughput is a measure of how much data can be delivered in a given period of time, and is closely related to the DRAM cycle time; a higher throughput means that a DRAM delivers more data per time interval. While the density of DRAMs has been quadrupling roughly every three years, neither their access nor their cycle times have improved as rapidly. Improving the latency and throughput of main memory is the focus of attention among memory system designers.

Page mode may reduce latency and increase throughput, but only if there is a lot of sequentiality in the memory reference stream; for multiprocessor systems, this is not true. Caches do a good job of isolating the processor from relatively sluggish main memory, but there is only so much a cache



[2] In a typical DRAM, such as the 4M-by-4-bit Toshiba Corp. part, the actual memory array in the lower right is accessed through paired successive row and column addresses. The row address causes the data in the row to be read into the sense-amplifier I/O gate from which the column address decoder selects the 4-bit word, or nibble, to be placed in the data-out buffer.

can do. The time it takes to service a cache miss is directly related to the main memory's latency so, with increasing processor speeds, cache misses have an ever greater impact on system performance, even when the hit-to-miss ratio is high.

BANKS AND BANDWIDTH. The most common method of increasing memory system throughput is interleaving [Fig. 4]. The idea here is to use not one, but several identical arrays of memory, or banks.

In its simplest form, interleaving spreads out the memory addresses so that adjacent addresses occupy adjacent banks. The number of banks used, N, is a power of 2. If an address yields a remainder of 0 when divided by N (or address modulo $N = 0$), then it resides in bank 0; if address modulo $N = 1$, then it resides in bank 1, and so forth.

The net effect of interleaving is to increase the memory bandwidth, or throughput, by a factor of N; N words are read each memory cycle instead of only one. The N words are stored in a register, freeing the memory banks to process the next access. If the memory addresses accessed are mostly sequential, this form of interleaving works well; if they are not, it does poorly.

Another form of interleaving, while more complex, works better for nonsequential accesses. As with the simple case, memory is divided into N modules and addresses are assigned to banks in the same way. In this case, however, the memory controller takes on the additional responsibility of scheduling accesses. It looks at each separate request and schedules it in such a way as to make maximum use of the data bus. The controller's objective is to overlap operation between memory banks as much as possible.

Even though interleaving is popular and helpful, it runs into several problems. For one, filling a wider bus may require too much memory. Also, to maintain the interleave, memory has to be upgraded in increments of N. Lastly, interleaving can result in bulky, complex memory systems.

While all these techniques have been used to improve systems performance, they will not be able to cope with the faster processors in the offing. A new memory architecture is needed, and in addition, the physics of the interconnections must be kept in view.

Designers of truly high-speed memory systems have to treat memory paths as transmission lines; their impedance has to be carefully controlled and paths have to be correctly terminated to reduce reflections. As for the parasitic capacitance and inductance of the I/O driver/receiver, the device packaging, and the printed-circuit board's traces, they have to be minimized and their effects taken into account.

High throughput demands high transmission rates. Since traditional TTL- and CMOS-level drivers and receivers cannot achieve the speeds necessary, new I/O drivers with low-voltage swings, carefully controlled slew rates, and the ability to drive a terminated bus are required.

In selecting a high-speed interface, a number of related factors have to be considered: the interface should be simple, effective, economical, widely supported, and easy to use, and should conserve power.

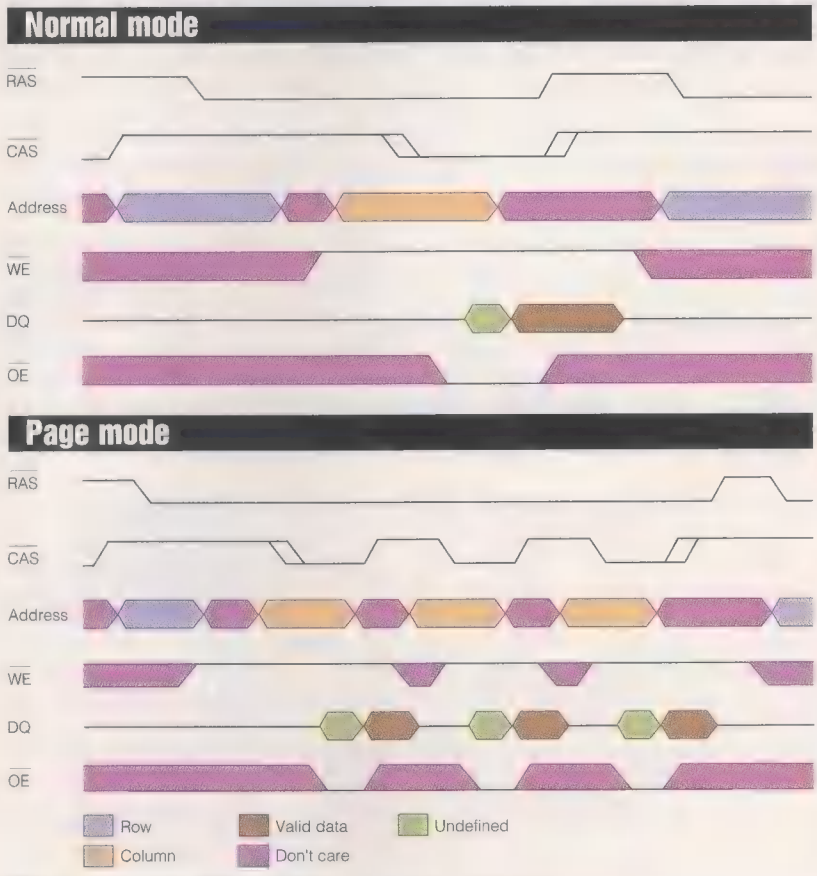
As speed increases, so, too, does the significance of schemes for distributing clock signals. Sophisticated techniques will have to be used to control clock skew—the different times of arrival of the same clock signal at scattered points in the system. Also, the delay introduced by the clock distribution network within each chip has to be controlled. Both skew and delay should be kept as low as possible.

New clock architectures should also be considered. Instead of distributing a central clock to all the chips in the system (global synchronization), it may pay to ship a copy of the clock along with the data (source synchronization).

MORE OPTIONS. Several new high-speed DRAMs solve some of the foregoing problems. Synchronous DRAMs resemble conventional DRAMs, and so are merely an evolutionary step in DRAM technology. They differ from early parts in that all inputs and outputs are referenced (synchronized) to the rising edge of a clock pulse. Another difference is that, when a read operation is performed, more than one word is loaded into a high-speed shift register; these words are shifted out, one word per clock cycle. As a result, synchronous DRAMs can have very high burst rates. (Note that some early synchronous DRAM designs use an internally pipelined design that operates on a single word only.)

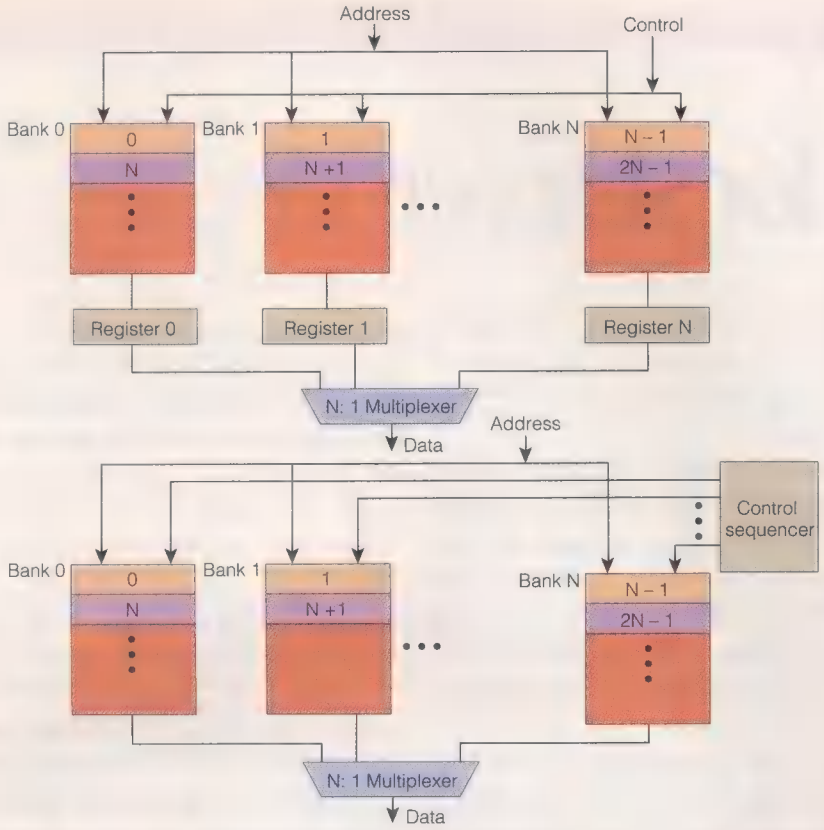
A synchronous DRAM running at 100 MHz has four times the bandwidth of page-mode DRAMs. However, access times are no faster than for conventional DRAMs. Some synchronous DRAMs do have a "wrap" feature, for servicing cache misses. They deliver a burst of perhaps four or eight cycles of data, with the addressed word appearing first, followed by the remainder of the block, and then wrap back around to the beginning of the block.

A memory system built out of synchronous DRAMs has a peak (ideal) bandwidth equal to the system's clock frequency multiplied by the number of data lines in the system's bus. While the bandwidth actually delivered will, of course, be less than this, the memory bandwidth is directly



RAS = row access strobe; CAS = column access strobe; WE = write enable; DQ = data input/output; OE = output enable.

[3] In a normal DRAM read cycle, data becomes valid only after both row and column addresses have been supplied. However, when all the data needed is stored in the same row, a page mode speeds matters by changing the column address only; after each change, the newly requested data is output and remains valid until the next column address is received.



[4] Interleaving divides main memory into blocks on the basis of address modules (the remainder when the address is divided by the number of banks, N, where N is a power of 2); because the banks can be accessed in overlapping fashion, throughput can be greater than for one bank by a factor of N. In the simplest scheme, all banks are activated simultaneously by a common control line, their outputs are stored in registers, and the registers' contents are consecutively multiplexed onto the system bus. If data is not stored and accessed from consecutive addresses, a more complex form of interleaving [bottom] allows each bank to be controlled separately so that the sequence in which the banks deliver data to the system bus can be tailored to optimize throughput.

proportional to the clock frequency.

To derive the maximum benefit from these DRAMs, therefore, a computer must be designed to run the memory system at a high clock rate. This requires very careful design, but the high burst rate of some synchronous DRAMs makes it possible to use narrower memory paths than would be required for conventional DRAMs.

At present, some vendors are sampling parts based on a synchronous DRAM architecture, and the Joint Electron Device Engineering Council (Jedec) is preparing a standard for them that will be available to any interested party.

ON THEIR OWN. The cached DRAM is a proprietary development of Tokyo's Mitsubishi Corp., from which samples are available. Because a cached DRAM has a small SRAM cache inserted between its external pins and an internal DRAM, accesses that hit a location in the cache are much faster than typical DRAM accesses. Also, the cache-fill bandwidth is very high because the bus connecting the SRAM and DRAM is very wide.

In system configurations where memory is connected directly to the processor, cached DRAM may replace the external cache. However, the memory controller must perform the functions of a cache controller and maintain a set of tag RAMs.

Another proprietary scheme, Rambus from Rambus Inc., Mountain View, Calif., offers a complete and radical solution to building a memory system. Its specification describes the protocol, electrical interface, clocking scheme, the register set, device packaging and pinout, and board layout.

Although its peak transfer rate is 500 megabytes per second, actual memory bandwidth is less because address, control, and data are all transmitted over the same set of wires. The bandwidth that is in fact achieved depends on two factors: the amount of data transferred during each transaction, and (since the scheme involves caching) the hit rate. The amount of overhead for each transfer is fixed, so bus efficiency increases with transfer size. Assuming a 100 percent hit rate, the peak read bandwidth for the 4.5M-bit part is about 360 Mbytes/s for 64-byte transfers; for the 18M-bit part, which is faster, it is about 400 Mbytes/s. Bandwidth decreases if the hit rate or transfer size decreases.

What does Rambus mean for the system designer? Because each chip is an independent entity, very few are needed to build a memory system and, because each chip has built-in decoding and hit detection logic, the memory controller can be simpler. If the hit rate is high enough, it may even be possible to connect the processor directly to memory and eliminate the cache. A special Rambus interface, containing the I/O drivers, phase-locked loop, and miscellaneous logic, is needed to interface to Rambus.

Since Rambus is theoretically a cookbook solution, the designer need not worry about the electrical interface and clock distribution issues; the details have all been taken care of. But because each device does much more than an everyday DRAM, Rambus DRAMs may cost more.

Rambus is a proprietary technology licensed to manufacturers of DRAMs and application-specific ICs (ASICs). Toshiba, Fujitsu, and NEC are currently sampling Rambus DRAMS. The Rambus interface cell is available from a few ASIC vendors, and Toshiba plans to make ASIC versions of the Rambus controller available.

RamLink is an attempt to take some of the work done for the Scalable Coherent Interface (SCI) and adapt it for use as a DRAM interface. RamLink will specify the protocol, required registers, and the electrical interface, which is a differential interface. While RamLink does not specify device pinouts or board layout, it is in many ways similar to Rambus; the chief difference is that RamLink is based on a ring, rather than bus, topology. The interconnections between each RAM are therefore point to point—and point-to-point connections can run faster than bused connections. The disadvantage of a ring topology is that the request and reply packets must traverse the entire ring. Each node on the ring adds some amount of delay, so the latency can be very high: RamLink allows up to 64 nodes.

It is anticipated that the RamLink specification will be an IEEE standard (P1596.4) when work is complete. No vendors currently offer a RamLink part.

BOTTOM LINE. Main memory is the single most expensive item in a computer system. The current cost of DRAM is about US $30 a megabyte. A typical PC today comes with about 4M bytes expandable to perhaps 16M bytes; a typical high-end workstation comes with about 32M bytes, and can hold up to 512M bytes. DRAMs are commodity parts whose price is driven by volume. Any DRAM enhancement must offer a clear benefit at a small price difference.

Any DRAM solution that can eliminate the need for a cache, yet cost little or no more than conventional DRAMs, could be of use in personal computers, low-end workstations, and other single-processor machines.

ABOUT THE AUTHOR. Ray Ng is a member of the technical staff of Sun Microsystems Inc., Mountain View, Calif., where he is involved with the development of memory systems for RISC-based workstations and future computer systems.

Fast DRAMs for sharper TV

New formats and features for digital television sets require inexpensive dynamic RAMs with extremely high throughput

Dynamic RAMs in the consumer world have two main digital-signal-processing applications: audio and video. The audio field is generally well served by commercially available devices. This is not nearly as true for video.

Computer graphics has been pushing the performance of dynamic RAMs (DRAMs) for years [Fig. 1]. That said, consumer applications such as high-definition TV (HDTV) ask much more of DRAMs than do personal computers and workstations. They also can have distinctive requirements slightly different from those of many other applications.

In television systems, memory is often used to store a full frame of video. As a bare minimum, therefore, the device must be able to absorb a digitized video signal at its incoming speed. While this seems a rather obvious and trivial request for today's video systems, for advanced applications such as HDTV, it is certainly not automatically fulfilled by a preexisting chip. Thus designers of video systems are keeping a watchful eye on what tricks DRAM makers are adding to their parts to improve overall throughput—not just access or cycle times, as is usually the case in other applications. It is throughput—the combination of data quantity and I/O speed—that is the essential concern for television systems.

Standard TV has several relatively undemanding applications for DRAM. Among those uses are teletext (the transmission of extra data at the end of a TV field) and conversion from 50 Hz to 100 Hz to reduce flicker, both of which are common in Europe. Additional burdens will be placed on memory by such more recently developed TV features as a picture within a picture, which displays a second TV channel as an inset on the screen, and by many planned picture-improvement algorithms, like those intended to reduce line flicker, large area flicker, or noise. Quite a few of the new picture-processing algorithms need random read/write capabilities for some, if not all, memory cycles.

Roelof H.W. Salters Philips Research Laboratories

TV MEMORY TODAY. As an example of the demands television currently imposes on memory, consider 50-to-100-Hz conversion. To double the display rate, the receiver must write one video frame into memory and display it twice, at twice the normal speed [Fig. 2]. While it is not essential that the conversion be done on the fly, as the signal comes in, it is most essential that not one bit of information be lost during the conversion process.

Typically, a buffer memory stores all the incoming data until it has been displayed twice. If the incoming video data rate is R, the buffer must have a total I/O rate of 3R. In Europe, 576-line pictures are projected onto a TV screen using an interlaced scan. A field (equal to half the picture or frame) is displayed every 20 ms. The first field contains the horizontal picture lines 1, 3, 5, . . .575, and the second field contains lines 2, 4, 6, . . .576 (unlike line-progressive-scan, where the lines are displayed in the normal order 1, 2, 3, . . .576).

The number of pixels in one TV field is thus equal to the number of pixels per line, 728, multiplied by 288 lines. With 12 bits per pixel (4:1:1 coding), the incoming data rate then is 720 by 288 by 12 bits per 20 ms, or 124 Mb/s. Since the outgoing data rate is twice as high, the total data throughput is 372 Mb/s, an imposing number even for today's dynamic RAMs.

> Even for today's TV, a standard dynamic RAM would need a throughput of almost 400 megabytes per second

One other problem remains. There has to be enough room for the new incoming data when it is arriving, yet none of the data already in memory may be disturbed for the first 10 ms. Only during the second 10 ms, when data is being read out for the second and last time, can data for the field currently being displayed be replaced with the incoming field's data. So during the first 10 ms at least, the memory must be big enough to contain all the data of the current field being displayed, plus the data already received for the next field.

The easy way out of these difficulties is simply to double the memory. With this scheme, it is possible to alternate between the two halves of the memory, writing in one half at a data rate of 124 Mb/s while reading out the other half at 248 Mb/s. If the two memory halves are indeed two separate memories, the memory speed requirement is relaxed to only 248 Mb/s.

If the memory were a single chip, the throughput required would not change, but having separate, independent read and write ports would ease the speed requirement. The original need for a 372-Mb/s read/write port, equal to a 21-ns cycle time for a byte-wide memory, would be reduced to 248 Mb/s on the read port, or a cycle time of about 30 ns for this hypothetical, byte-wide part. Obviously, I/O ports with excessively high data rates make life more difficult in the TV world.

Of course, doubling the memory size is more than the minimum theoretically necessary to implement a conversion scheme. But the cost of realizing the more complex addressing schemes that result from using a memory with, say, 1.5 times the number of bits of a TV field, is likely to offset the cost of the additional memory. And cost is a primary consideration in consumer electronics.

A further improvement in TV picture quality is expected when a shift is made from interlaced scan to a line progressive scan in which all 576 lines are displayed in 10 ms. Again, the required performance and size of memory increases.

In the simpler applications, like 50-to-100-Hz conversion, the memory is written to and read from in a very ordered manner, so that dedicated memories with simplified addressing capabilities can be used.

For straightforward field memories with no need for random access, the market offers a variety of DRAMs with serial input and output ports, usually referred to as video DRAMs. Video DRAMs work at the speeds needed for today's TV and, since they are not designed with random access, page mode, or other such features, they can be very cost-effective. However, these parts do

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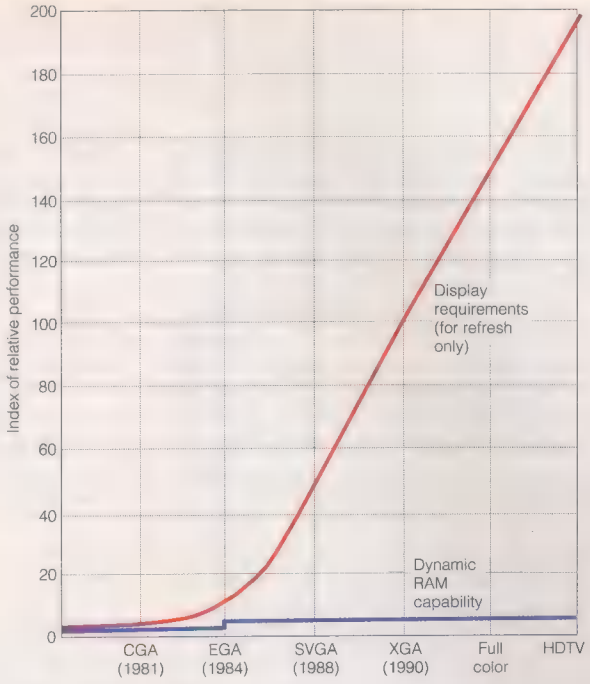
[1] Computer graphics has been demanding more of memory systems for the last decade: with each new generation of display technology, performance requirements have at least doubled. But high-definition television requires even greater capabilities of dynamic RAMs. As of now, requirements for the two endeavors seem to be diverging, but ultimately multimedia users will expect computer graphics displays to look and act more like full-motion video.



not yet meet the maximum bandwidth requirements for a full-fledged HDTV frame memory.

HIGH-DEFINITION DRAM. For HDTV in Europe, the picture size will be 1152 lines by 1440 pixels. Therefore, the field size for interlaced HDTV would be 576 by 1440 pixels, and each pixel will use 16 bits (4:2:2 format). Thus an HDTV set will need to store one field of 576 by 1440 by 16 bits (which works out to about 13 Mb) every 20 ms and a whole picture needs about 26 Mb. The obvious solution is to write in one picture while reading the previous out of another section of the memory; for this, the memory needed exceeds 32 Mb.

It is expected that there will be a few generations of HDTV. The first will use a minimum of the mentioned features and therefore need "only" some 9 Mb for a signal decoder that conforms to the high-definition multiplexed analog component (HD-MAC) standard. Adding features to reduce large area and line flicker leads to the 26-Mb requirement.

Regardless of the total bits stored for use in these picture improvement techniques, the incoming data rate is 13 Mb every 20 ms, yielding a throughput of 650 Mb/s, or 83 Mbytes/s. Reading out every 10 ms requires a throughput of 166 Mbytes/s.

A single, 8-bit-wide memory chip, if used, would have to write once and read twice every 12 ns. For ■ single-port DRAM, this would mean 4-ns read and write cycles; ■ multiport DRAM would need to read in 6-ns and write in 12-ns cycles. In either case, current DRAMs cannot operate anywhere near these speeds. Whether the memory system employs one or more chips, the wider the total I/O bus, the less the demand on the cycle times.

The total memory size required, however, is within the size of DRAM chips already being sampled or soon to be available. So while the memory industry can provide ■ one-chip solution to the TV designers' problems in terms of memory size, it cannot do so in terms of throughput.

A memory system could be built using familiar 1M-bit chips—say, 32 chips each with ■ 256K-by-4-bit architecture—and with buses 64 bits wide so as to support both reading and writing. With a bus eight times as wide, the read throughput required is only one-eighth the speed of a single-chip system. So the read cycle time is then 48 ns, which is within reach of any standard DRAM's fast access modes—page mode, for example.

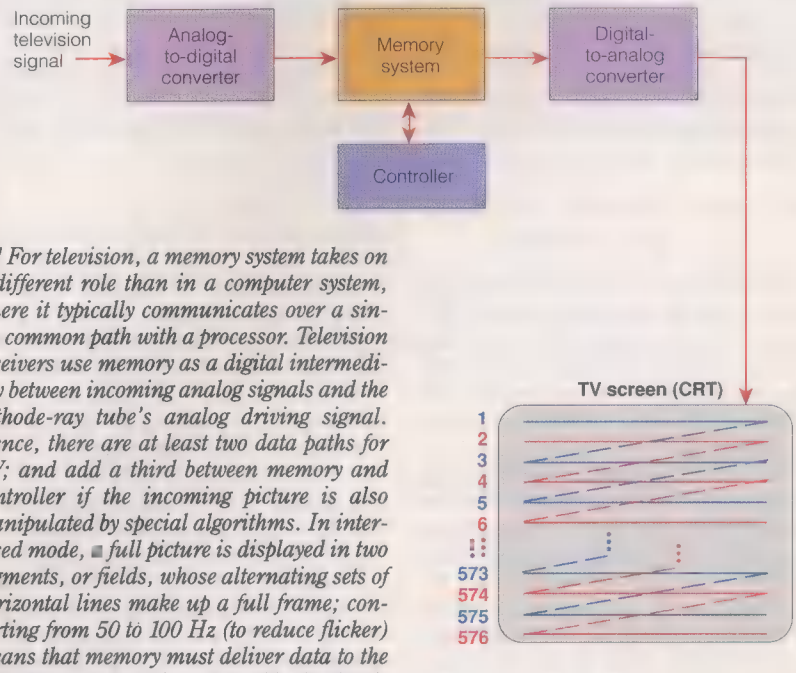
This does not signal the end of the system requirements, however. The switching and the multiplexing and demultiplexing circuitry needed in this case adds quite a large number of fast logic chips.

This system does solve the technical problem in terms of both memory size and access to the data, but at literally too steep a price. The use of 32 memory chips and additional high-speed logic would result in a system whose costs would be prohibitive for the consumer market.

RANDOM REQUIREMENTS. The fast access modes of standard DRAMs have some shortcomings; they are, at best, random access within the "page," that is, within a limited set of addresses. Beyond that address range, only the slower, normal-mode access times of the DRAMs are applicable.

Because of this constraint, TV system designers must carefully evaluate whether or not the addressing capabilities of a proposed DRAM system can meet the data requirements of the picture manipulation algorithms they want to build into ■ TV system. To support an algorithm requiring totally random access, DRAMs would have to have access cycle times equal to the page mode cycle times just mentioned. This would have the effect of tripling the required DRAM performance.

Dedicated systems built with video DRAMs —or multiport DRAMs, as they are called in the Joint Electron Device Engineering Council's standard terminology—are an alternative to standard DRAMs. Multiport DRAMs differ from standard DRAMs mainly in having, as the name says, more than one I/O port. But while ■ memory can have several ports in theory, in practice most of



[2] For television, a memory system takes on a different role than in a computer system, where it typically communicates over a single common path with a processor. Television receivers use memory as a digital intermediary between incoming analog signals and the cathode-ray tube's analog driving signal. Hence, there are at least two data paths for TV; and add a third between memory and controller if the incoming picture is also manipulated by special algorithms. In interlaced mode, ■ full picture is displayed in two segments, or fields, whose alternating sets of horizontal lines make up a full frame; converting from 50 to 100 Hz (to reduce flicker) means that memory must deliver data to the cathode-ray tube twice, at double the data's incoming speed.

The next PC could be the TV set

During the 1980s, the growth in sales of memory chips was mainly due to adoption of personal computers by businesses large and small. In the latter half of the 1990s, the most important market for those chips appears likely to be television. In that era, it is anticipated that new television broadcast capabilities—higher definition, better reception, and new applications—will win consumers over to purchasing new TV receivers that make use of the improvements.

The potential market for high-definition TV (HDTV) simply dwarfs that for PCs. According to the Television and Cable Factbook No. 57 (Warren Publishing Co., Washington, D.C., 1989), there were over 600 million television receivers in use worldwide in 1989, about half of which were color. In contrast, estimates of the current installed base of personal computers range from 80 million to 100 million.

Not only will more TVs than PCs be sold, but each receiver will use more memory than the typical PC. Today, most PCs come with 2M–4M bytes of RAM, expandable to 8M bytes. At a minimum, the new sets will need 9M bytes, and sets with all the new features will require at least 32M bytes. Further, HDTV will give rise to demand for new videocassette recorders, video cameras, and studio, cable, and broadcast equipment, all of which will require RAM.

The market for such receivers will begin to open up in the United States after June 1993, if all goes according to plan. In July of 1991, the Advanced Television Test Center in Alexandria, Va., began testing the various proposals for HDTV. The backers of a particular HDTV scheme must deliver and maintain an end-to-end TV system (transmitter to receiver) that operates in real time without any simulations. The Center's laboratory checks for interference from cochannels (different services in different communities that use the same channel), adjacent channels, and aircraft. In addition to quantitative analysis of a system's performance, the center makes tapes of the transmitted programs as they appear on the receivers for subjective evaluation by a lay audience. This testing should be completed this year, and the results forwarded to the Federal Communications Commission's Advisory Committee so that it will be able to make an evaluation and recommendation to the agency by next summer.

The first system that was tested by the Center is called Advanced Compatible Televison (ACTV). It is sponsored by North American Philips Consumer Electronics, Thomson Consumer Electronics, the National Broadcasting Company, and the David Sarnoff Research Center. In this system the signals for both the advanced capabilities and the standard NTSC signal are transmitted in the same 6-MHz band. The group also supports a simulcast system, in which two separate signals, one with a 6-MHz band and another with a 4-MHz band, respectively supply the standard TV aspect ratio (4:3) part of the broadcast and the pieces, or side panels, necessary to expand to HDTV's aspect ratio (16:9).

On the other side of the Atlantic, the European Commission has issued a directive encouraging the use of D2-MAC. This scheme for high-quality, direct broadcast by satellite (DBS) of current European TV formats is based on the use of multiplexed analog components (MAC) in which separate analog signals for chrominance (color value) and luminance (brightness) are compressed and multiplexed, along with digitally sampled audio signals. The satellite transponders digitally store and reassemble the signals to provide a high-quality picture. Philips of the Netherlands, France's Thomson, and Finland's Nokia are major proponents of D2-MAC.

HD-MAC, an HDTV DBS system compatible with D2-MAC, is under development as part of the European Commission's Eureka project; Philips, Thomson, and Germany's Siemens are the principal companies involved. The plan for HD-MAC is to double the number of lines per frame and increase the aspect ratio from 4:3 to 16:9; initially, interlacing will be used when broadcasting signals on a 27-MHz channel.

The HD-MAC system deals in a unique way with a problem found in other DBS systems, such as the early multiple-sub-Nyquist-sampling encoding (MUSE) system employed in Japan, namely, how to accommodate motion. Because MUSE builds a full-resolution image from three sets of information, each sent once every three frame periods, motion in the image smears it. While this smearing is not noticeable for minor movement within an image, it is noticeable if there is a great deal of motion, for instance, when the camera is panned.

In the HD-MAC system, this problem is dealt with using a new three-part encoding and decoding architecture called digitally assisted television (DATV). The encoder differentiates between three degrees of motion: extremely slow or stationary scenes in which the picture need only be updated every four frames (80 ms); moderate motion which requires an update every two frames (40 ms); and fast motion needing single-frame updating (20 ms).

A motion processor determines the type of encoding needed for a scene and switches in the correct encoder. It also generates a special DATV signal, which is transmitted along with the picture information to the receiver so that it can properly decode the incoming signal. This DATV signal, transmitted during the 2-ms vertical blanking period, has a maximum practical bit rate of 960 kb/s.

Any one who doubts that there is truly a market for HDTV need only look at the experience of the Japanese. Research conducted in Canada and the U.S. in 1987, using the MUSE satellite broadcasting system developed by Japan Broadcasting Corp. (NHK), Tokyo, showed that there was a strong preference for HDTV; observers indicated that they would be willing to pay more for pay-per-view movies broadcast in that format. What's more, Japanese consumers purchased over 100 000 converters for letting NTSC-compatible receivers pick up MUSE DBS signals in 1988—a year before regular broadcasts started.

HDTV was first developed in 1968 at NHK's Technical Research Laboratories, and NHK has been developing MUSE for over 20 years. Actually a family of proposals, various forms of MUSE cover every aspect of high-definition recording, transmission, reception and playback. One form, Narrow MUSE, has been tested by the Advanced Television Test Center as a possible U.S. standard, even though it is not compatible with any previously existing TV format.

—Richard Comerford

the devices seen until recently have had only two I/O ports: one a random access port, and the other a serial access port.

DRAMs of this kind reduce the bandwidth problem by allowing simultaneous read and write accesses to storage. Still, they are far more expensive than standard DRAMs, and it seems unlikely that the current type will prove to be cost-effective for video memory applications.

Conceived with computer graphics applications in mind, they have many built-in features that make sense chiefly in that environment. For instance, the standard video DRAM's two I/O ports can be used at the same time. In TV applications, however, only one input port and one output port need be independently active at the same time; there is no need for two inputs or outputs at the same time.

Because, after all, it is ultimately the consumer who will decide which features will be common in all HDTV sets, it is not yet clear which of the potential picture-improvement algorithms will actually be implemented, and some of these features may only be made available in high-end receivers.

Depending on what the marketplace chooses, the TV requirements for DRAM may vary between some 9 Mb to over 32 Mb. At present, it does not seem likely that one type of DRAM will cover all the technically feasible applications.

TV applications present dynamic memory makers with a challenge that is not quite the same as the application problems they have been solving up to now. Maybe dedicated DRAMs will appear that combine just those features needed in TV applications with the very high-speed capabilities that are essential.

ABOUT THE AUTHOR. Roelof H.W. Salters is chief scientist at Philips Research Laboratories, Eindhoven, the Netherlands. He has worked in circuit design, mainly digital logic and memory circuits, during most of his career. He has been with Philips all his professional life, spending a number of years with Signetics Corp., Philips' U.S. semiconductor affiliate in Silicon Valley in California. He is currently a task group chairman in the Joint Electron Devices Engineering Council (Jedec) JC-16 committee on low-voltage standards and a member of the Jedec JC-42.3 committee on RAM. Salters recently was coauthor with Betty Prince of Texas Instruments Inc. of an article, "ICs going on a 3-V diet," in the July 1992 issue of *Spectrum* [pp. 22–25].

A new era of fast dynamic RAMs

Chip makers are turning to innovative circuit designs to bring inexpensive dynamic memories up to speed

Way back when, the microprocessor's need for data outstripped the rate at which dynamic RAM could access the information; so to catch up, system designers turned to cache subsystems based on static RAM. But static RAM, though faster, is also the costlier form of chip memory. Now an alternative has arrived. Until recently, only a few suppliers focused on the high-speed dynamic RAM market; now many are developing high-speed I/O concepts, in a move away from the high-density, low-speed memory-chip-as-commodity market. For system designers, that means fast, inexpensive new dynamic RAMs (DRAMs) are here, while static RAM (SRAM) is being displaced or relegated to the DRAM chip.

For example, three generations (256K through 4M bits) of address-multiplexed DRAMs with row address access times as short as 40 ns have emerged from NMB Semiconductor Co. While the Tateyama, Japan, company employed standard CMOS technology, Tokyo's Hitachi Ltd. used the more complex and expensive biCMOS process to extract a 25-ns access time from a 1M-bit-by-1 nonmultiplexed (broadside-addressed) DRAM.

Seldom do these speed-optimized devices require larger chips to achieve their higher performance. Though Hitachi's new fast DRAMs are fabricated with specially optimized processes, others resort to imaginative circuit designs to obtain high speed.

Several new chips turn the wide data buses within DRAMs to advantage; on most of them, 1024 to 4096 memory locations may be accessed in parallel. Examples are cache DRAMs, enhanced DRAMs, synchronous DRAMs, and Rambus DRAMs, all described later in this report. While all these ICs capitalize on wide on-chip buses, they vary greatly in their die sizes, terminal characteristics, and performance benefits [Table 1, p. 44].

Fred Jones United Memories Inc.

FIRST APPLICATION. Video was the high-data-rate application that spurred the development of application-specific DRAMs that utilize wide on-chip buses. Video RAMs take wide data fields within the addressed row and transfer them, in parallel, into parallel-to-serial registers. When loaded, the registers independently clock serial data out of the serial port to refresh the video screen, while the processor or graphics processor is accessing the random access port to update the image.

Often, split registers load half the serial register for the on-chip video port, all the while clocking serial data out of the other half-register. A split register thus loads data into the serial registers without interrupting the data stream from the video RAM's serial port.

Other features on video RAMs, such as block and flash writes, simplify and speed up many graphics operations. In general, the dual-port architecture of video RAMs is their prime attraction, but they rarely demonstrate blazing speed on either of the I/O ports. Rather, the high video pixel rate is produced by accessing data broadside from the serial ports of several chips and by boosting the data rate with high-speed parallel-to-serial shift registers or other bit acceleration techniques.

> Once considered too slow for high-performance applications, dynamic RAM can now replace fast but expensive static RAM

WIDE BUSES. Like video RAMs, cache DRAMs and enhanced DRAMs fill on-chip caches from their internal buses. Their SRAM caches are integrated into a standard CMOS high-density DRAM chip, yielding a much higher data transfer rate between dynamic memory and static RAM cache than if they were on separate chips. The on-chip cache is also more effective and less expensive. These single-chip cached dynamic RAMs produce full output voltage swings, either CMOS- or TTL-compatible, but may also use limited-swing I/Os in the fiture.

The enhanced DRAM from Ramtron Corp., Colorado Springs, Colo., uses 8K bits, distributed on chip, of static RAM cache (2048 bits are accessible during a given cache read) ["Enhanced dynamic RAM," p. 49]. The cache is direct-mapped and row (address) associative. Since 2048 bits are transferred in parallel (from DRAM array to cache) when the cache is loaded, the fill bandwidth per device is 7.3 gigabytes per second.

Access time for a cache hit is 15 ns (giving a total cycle time of 15 ns), and for a cache miss, 35 ns (65-ns cycle time). Read or write burst cycle time is 15 ns. All memory cycles are asynchronous. Refresh cycles and precharge operations can be hidden during cache read operations.

A write-through cache is used to maintain coherency between cache and main memory: data is written to the main memory array through the cache for a cache hit, but written to the array directly for a miss. With the enhanced DRAM, this practice incurs none of the delay normally associated with write-through architectures, since both the memory write and cache write operations together require only a 15-ns write cycle.

SPLIT SECOND. Cache can be read immediately after a write hit (write to cache), but a write to read latency (30 ns maximum) occurs when a read miss or write miss (data not in cache) occurs after any write operation. This seldom affects system performance because of traditional bus protocol limitations. With write-through cache, writes (except for posted writes) occur in real time, without the additional latencies associated with copy-back cache.

The cache DRAM from Mitsubishi Electric Corp., Tokyo, like Ramtron's enhanced DRAM, utilizes on-chip cache, but in a different role ["Dynamic RAM as secondary cache," p. 49]. The Japanese DRAM contains two 8K-bit sections of localized on-chip static RAM (256 rows of 16 four-bit words); each may be configured either as direct-mapped, two-way set-associative, or as four-way set-associative. In a cache transfer, 64 bits (16 by 4) are moved in parallel, giving the cache DRAM a cache-fill bandwidth of 114 megabytes per second.

For cache hits, access time is 10 ns (10-ns cycle), while for cache misses and direct array access, it is 70 ns (280-ns cycle time for cache operations, 140 ns for direct array

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High-speed dynamic RAMs—a comparison

Type of dynamic RAM	Enhanced	Cache	Synchronous	Rambus
I/O width, bits	X1, X4	X4	X4, X8, X9	X8, X9
Data rate, single-hit, MHz	67	50–100	50–100	500
First-access latency Cache/bank hit, ns Cache/bank miss, ns	 15–20 35–45	 10–20 70–80	 30–40 60–80	 36 112
Cache-fill bandwidth, Mbytes/s	7314	114	8533[a]	9143[a]
Cache/bank size, bits	2048	8192	4096[a]	8192[a]
Area penalty, percent[b]	5	7	5–10	10–20
Output level	CMOS/TTL	CMOS/TTL	CMOS/TTL, GTL/CTT	600-mV swing, terminated
Access method	Asynchronous, DRAM-like	Synchronous, proprietary	Synchronous, pulsed/RAS	Synchronous, proprietary
Access during refresh	Yes	Yes	Undecided	No
Pin count/package	28/SOJ	44/TSOP	44/TSOP	32/VSMP
Density, bits	4M	4M	16M	4M

CTT = center-tap termination; GTL = Gunning transceiver logic; RAS = row access strobe; SOJ = small-outline J-lead package; TSOP = thin small-outline package; VSMP = nonstandard vertically mounted package.
a Synchronous and Rambus DRAMs store data in sense amplifier latches, not in separate synchronous RAM cache.
b Area penalty is relative to the manufacturer's standard die size, so that the figures are not directly comparable.

accesses). All memory cycles are synchronous. Refresh cycles and precharge operations can be hidden during cache read operations.

The cache DRAM uses fast copy-back to maintain cache/main memory coherency. If a cache miss occurs, the old data is moved into an on-chip temporary buffer until the new block is moved, in 70 ns, from the DRAM into the cache. The old block, if it needs updating, is moved to main memory, updated, and returned to cache while the processor is accessing the cache. Except for multiple back-to-back misses, this method hides the latency of write-back cycles and takes one-third the time of traditional write-back methods.

NEW CLASS. Meanwhile, a new class of memory chips, synchronous DRAMs, is being developed by several suppliers ["Synchronous dynamic RAM," pp. 44–48]. The synchronous DRAM bursts data sequentially from its wide internal bus at synchronous clock rates of 50 to 100 MHz. Many believe it will become the next standard DRAM.

Synchronous DRAMs provide high sustained data rates, but impose long delays for single random reads or writes. All memory functions of the synchronous DRAM are timed from the rising edge of a master high-speed clock (up to 100 MHz). Pipelining ensures fast, sustained sequential accessing and queued writing. Synchronous DRAMs are optimized for sequential data transfers (sequential binary Intel burst sequences) rather than random access. Precharge operations can be hidden by using interleaved accesses to separate memory banks within the synchronous DRAM. Depending on the performance range of the synchronous DRAM, I/O levels will be either full swing (CMOS/TTL) or restricted swing (Gunning transceiver logic, called GTL, or center-tapped termination, called CTT).

Rambus DRAMs, based on a bus concept developed and licensed by Rambus Inc., Mountain View, Calif., are being developed by several large manufacturers ["A fast path to one memory," pp. 50–51]. They share some characteristics with cache, enhanced, and synchronous DRAMs. Rambus DRAMs are intended for use in a very controlled and specifically defined Rambus environment, in which both transitions of a 250-MHz clock are used, for an effective clock rate of 500 MHz (clocked at a transition every 2 ns). The serial burst data rate is expected to be at the effective clock rate—that is, 500 megabytes per second.

This data rate is phenomenal for DRAM. But it applies to data packets once they start being transferred—it does not include the delay associated with the request protocol, particularly when a miss and re-request occur; these operations take a disproportionately long time.

Moreover, the transfer time is 2 ns within the Rambus environment only; it applies to the transfer of data between master and slave portions of the local memory bus, and not between the Rambus environment and the subsystem (a central processing unit or graphics processor, say) that uses the high-speed data.

Even so, system and equipment designers have a far wider choice of memory devices than they did just a year ago.

Synchronous dynamic RAM

Betty Prince, Roger Norwood,
Joe Hartigan, Wilbur C. Vogley
Texas Instruments Inc.

Data rates of 500 megabytes per second are expected for ■ dynamic RAM with ■ new architecture, new interfaces, and ■ new name: the synchronous dynamic RAM. In other words, the 100–200-MHz microprocessor of the mid-1990s could function nonstop if this kind of dynamic RAM (DRAM) were used for main memory. In addition, in simple cases, main memory might once again handle special functions like graphics, which currently need specialty DRAMs to achieve high enough data rates.

Yet the synchronous DRAM is an evolutionary approach to high-speed memory, in that it ties together, in a single device, many of the diverse techniques developed over the years to augment memory transfers. The plan is for it to become a multi-sourced, commodity chip.

SPEED MISMATCH. Standard DRAMs and the new microprocessors have increasingly diverged in speed. Basic DRAM architecture has not changed since the early 1970s, whereas design and architectural innovations have improved microprocessors to the point where speeds of 500 MHz or more look possible by the end of the decade. DRAMs, on the other hand, currently take about 60 ns to access a row address, or 30 ns from address to data available in page mode, which is about a 25-MHz cycle time. The problem is compounded by the increasing density of dynamic RAMs, which further adds to the time needed to access the total memory through a memory bus of a given width.

CHIP SOLUTIONS. Still, as DRAM chips have become larger, chip-level solutions have begun to appear. The cache, for example, can be included on the DRAM. Fast-access modes such as page mode, static column mode, or nibble mode have helped to nearly double basic DRAM speed. Page and static column modes work by keeping the active row data latched in the sense amplifiers, and merely selecting new random column addresses. Nibble mode uses wider internal architectures (by 4) and fast registers to make ■ 4-bit parallel-to-serial conversion. The result is fast access to 4 consecutive bits after a random address.

Although these modes can enlarge DRAM bandwidth to twice its normal, non-mode width, they still fall far short of today's processor needs. Wider external data buses (8 or 16 bits wide, for example) can also allow more information to be retrieved from the DRAM on a single access. The penalties here are larger chips and packages and greater DRAM output noise, all of which tend to slow down the read access.

NONPROPRIETARY. In the synchronous DRAM, many manufacturers, including Texas Instruments, Samsung, Hitachi, Toshiba, Mitsubishi, and NEC are addressing these speed concerns in an evolutionary, nonproprietary approach. Initially, they are developing synchronous DRAMs of 16M-bit capacity. These are currently being considered for open standardization in the Electronic Industries Association/Joint Electron Devices Engineering Council (EIA/Jedec) JC42.3 DRAM Standards Committee. (While synchronous static RAMs have been around for some years, the idea of using a dynamic RAM synchronously has only recently gained acceptance.)

Historically, DRAMs have been controlled asynchronously: the processor presents addresses and control levels to the memory, indicating that a set of data at a particular location in memory should be either read from or written into the DRAM (for a write, the processor also presents the data it wants written). After a delay—the access time—the RAM either writes the new information from the processor into its memory or else provides the information on its outputs for the processor to read.

During the access-time delay, the DRAM performs various internal functions, such as activating the high capacitance of the word lines and bit lines, sensing the data, and routing the data out through the output buffers. The delay creates a wait state for the processor; it simply waits for the RAM's response, and the entire system slows down as a result.

Under synchronous control, on the other hand, the DRAM latches information in and out under the control of the system clock. The processor drops off the instructions for the DRAM in a set of latches, which stores the addresses, data, and control signals on the DRAM inputs until the memory can process the request. The DRAM responds after a set number of clock cycles, which can be programmed by the user in a special configuration cycle.

NO WAITING. Since the processor knows how many clock cycles it takes for the DRAM to respond, it can safely go off and do other tasks while the RAM is processing its requests. An example is a DRAM that has a 60-ns read delay after initial addressing and is operated with a 10-ns (100-MHz) clock. If the RAM is asynchronous, the processor waits the full 60-ns access time for the information. But if the DRAM is synchronous, the processor can strobe the addresses into a set of input latches and do other tasks while the memory does the read operation. Then, when the processor clocks the outputs of the RAM six cycles (60 ns) later, the data it wants is there.

In the synchronous DRAM timing diagram, the row address is strobed in on the rising edge of the system clock, activating a row or word line of memory bits. A column address is then clocked in after three clock cycles (30 ns), sufficient time to activate the word line. The byte of data then appears on the outputs after three more cycles (another 30 ns) to decode the new address and get the data from the sense amplifiers through the output buffers. Six clock cycles after the row address has been clocked in, the processor can expect the requested information from the output buffers of the synchronous DRAM.

The architecture of the synchronous DRAM can further shorten its average access time by pipelining addresses. The input latch stores the next address the processor will want while the RAM is operating on the previous address. Normally the addresses to be accessed are known several cycles in advance by the processor; therefore, after the address for the first access has been sent and the RAM has started working on it, the processor can send the following address to the input latch, so that it is available as soon as the first address has moved on to the next stage of processing. The processor need not wait a full access cycle before starting its next access to the DRAM.

Various techniques can also be used inside the synchronous DRAM to hide the components of the internal timing delay. The address setup time and word and bit line precharge time can be eliminated after the first access by using a burst mode, in which a series of data bits can be clocked out rapidly after the first bit has been accessed.

The burst mode in the synchronous DRAM is similar to the old nibble mode, in which 4 bits of sequential data are provided in rapid succession without inputting new address information to the DRAM—but now as much as a full page of data can be provided [Fig. 1].

Burst mode is only useful if all the bits to be accessed are in sequence and in physically the same row of cells as the initial access. Likely applications include high-speed memory functions such as video support requiring 100-MHz data rates.

Burst mode can be combined with a "wrap" feature. The wrap gives access, for example, to strings of bits stored both before and after the initial bit location in rapid succession after the initial access. This feature is useful for cache filling, since the most likely bits to be wanted next are those physically close to the current bit. The user can program both the type of wrap and the number of bytes available on each wrap.

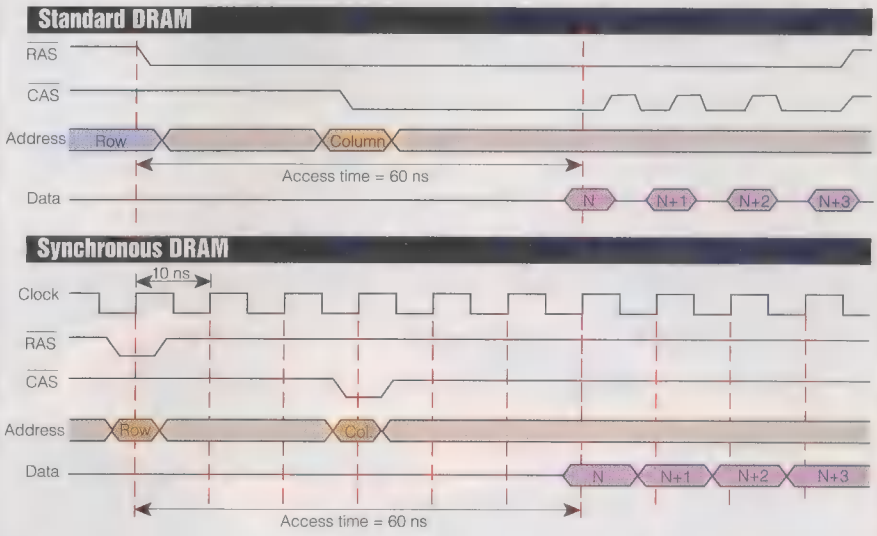
If data from different rows is needed, it is still possible to hide some of the row precharge time if the two rows lie in different banks. With the synchronous DRAM, the multiple-bank interleaving previously done at the system level may be moved onto the chip. Then one bank can be precharged while another is being accessed. An example is the "nibbled-page" architecture of Tokyo's Toshiba Corp., in which the data from 8-bit sections of different columns is interleaved on-chip to give byte-level random access at a 100-Mb/s rate.

Another advantage of multiple-bank synchronous DRAMs is that the active rows (potentially one in each bank) may serve as a cache. In more detail, once a given row in a given bank is accessed, it is held active and may be accessed again simply by supplying a new column address. This method has been used in page-mode devices, but had only limited success because only one row in an asynchronous DRAM could be held active.

ADDING ASSETS. All these features—burst and wrap modes and interleaved banks—can be combined on a single synchronous DRAM that runs at up to 400–500 MHz. And still more features may be added. For example, a data mask control can be used as an enable/disable pin to ignore inputs or turn the outputs off for a single clock cycle. This could be useful, especially in write cycles, if the user wants to access a string of bits, but not all in the string.

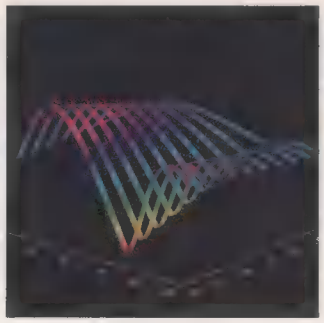
Another feature, clock enable/disable, turns off the system clock inside the RAM, thereby suspending the device in its current state, or puts it into low-power standby mode, saving energy in battery-powered equipment.

Synchronous DRAMs need a refresh cycle, since they are still composed of dynamic cells that lose their charge. But another option, self-refresh, appears on many of the newer byte-wide DRAMs. This new, simpler refresh mode is completely controlled on the chip and retains data in a low-

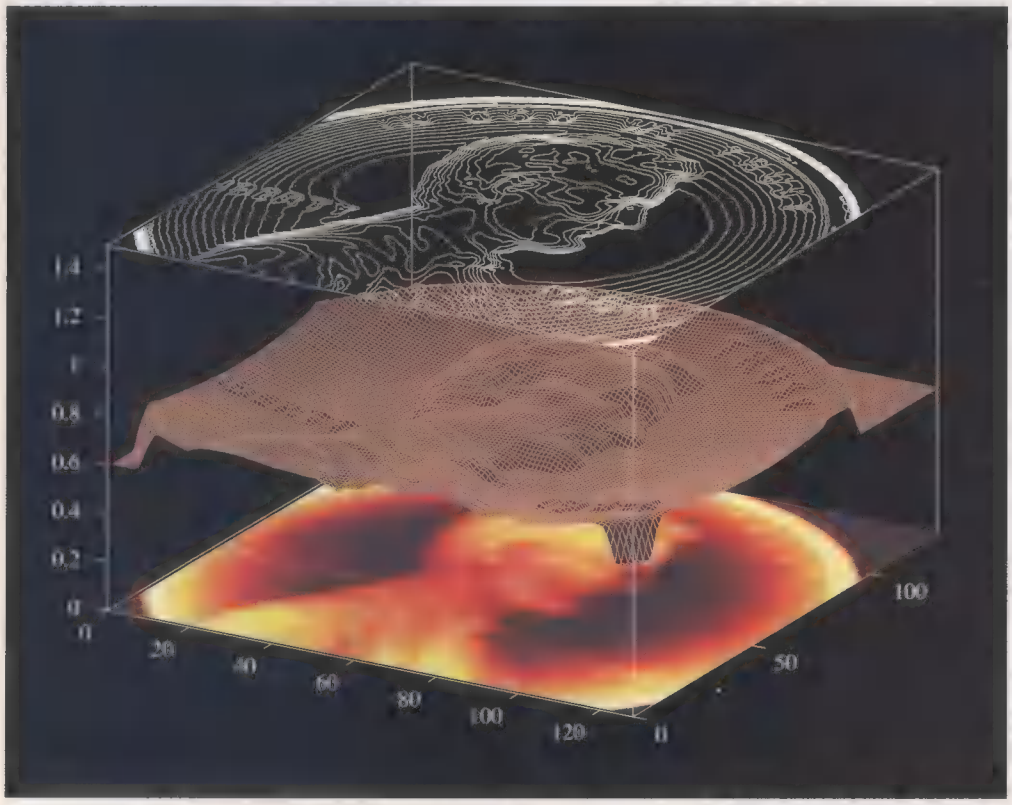


[1] In nibble mode on an ordinary DRAM, 4 bits of data from locations N, N+*1,* N+*2, and* N+*3 appear after location* N *has been addressed. Burst mode in a synchronous DRAM, however, can produce as much as a full page of data (typically 512 bits per output) after only* N *has been addressed.*

Frequency responses of a family of control systems, modeled, simulated and visualized in MATLAB 4.0.



We see your expectations of visualization and we raise them.



Three views of the surface height of a penny show user customizable object-oriented graphics in MATLAB 4.0. Data courtesy of NIST.

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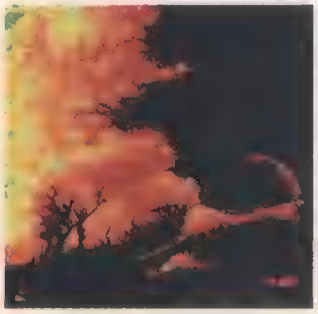

Image representation of Southeastern New England altitude data created in MATLAB 4.0. Data courtesy of NOAA.

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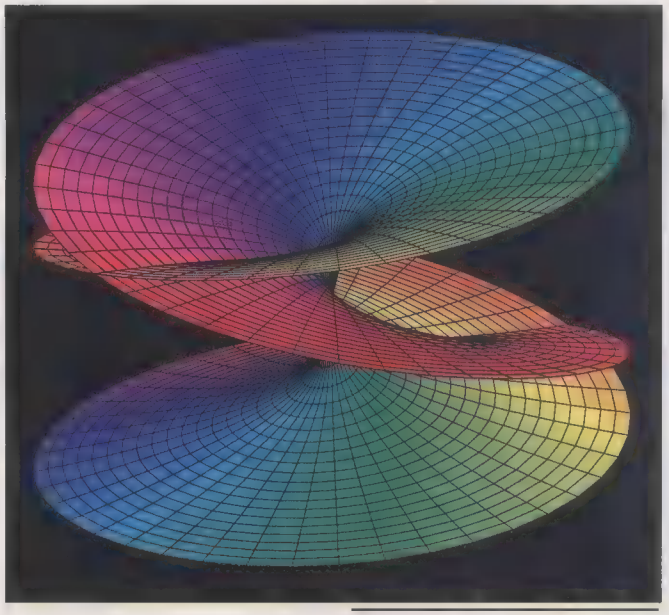

Riemann surface of the complex cube root function shows the capability of MATLAB 4.0 for mathematical visualization

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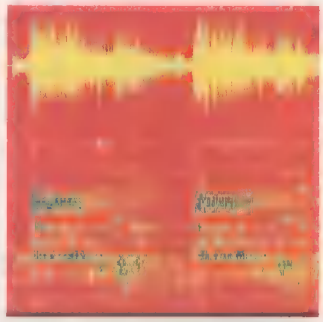

Spectrogram of Handel's Hallelujah Chorus, *computed and displayed with MATLAB 4.0 and the Signal Processing Toolbox.*

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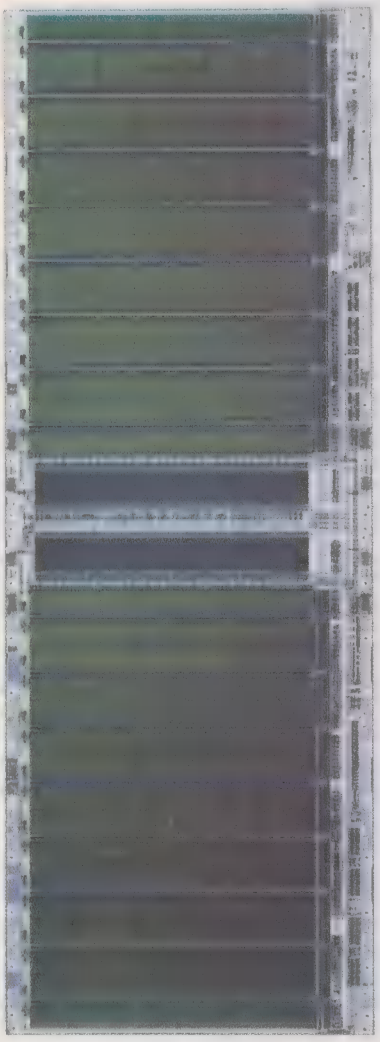
power mode. The self-refresh option is expected to be available on synchronous DRAMs from many vendors.

The final speed attained by this kind of DRAM in a system depends not only on its internal architecture but also on the interface signal levels it uses. A 5- or 3.3-V interface can function smoothly in, say, a desktop computer running at 50 MHz. If, however, these same interfaces, with their relatively large 2-V output swings (0.4 V low to 2.4 V high), run in a 125-MHz system, unterminated lines longer than a few centimeters could cause delays. Therefore, higher-speed synchronous DRAMs will have low-swing interfaces such as Gunning transceiver logic (GTL) or center-tap-terminated (CTT) ["Fast interfaces for DRAMs," pp. 54–57] to compensate for transmission-line effects.

SHORTER LEADS. The high speed of synchronous DRAMs influences their packaging. Most appropriate for them are new miniature packages such as the thin small-outline package (TSOP) or various vertical surface-mount packages. These reduce the effective length of the package wiring and leads, and devices may be tightly spaced on a circuit board.

Advances in fast DRAM architecture, high-speed interfaces, and miniature packaging combine in the synchronous DRAM into a widely sourced device type that could become the next-generation commodity DRAM. Whether the promise is fulfilled depends on several factors: producers must standardize their products and they must produce them in the high volume needed to bring costs down. No less important, many mainstream DRAM manufacturers must offer synchronous DRAMs so that users may have alternative sources to rely on.



[2] A cache DRAM contains static RAM in two shorter banks at center of die.

Dynamic RAM as secondary cache

Charles A. Hart
Mitsubishi Electronics America Inc.

Virtually all future microprocessors will have a first-level cache memory on chip, where it boosts efficiency by allowing access hits 80–90 percent of the time. But as processor clock frequencies rise, so does the deleterious effect of cache misses on system performance. This is where cache DRAM [Fig. 2] can play a key role: it provides a second-level cache that complements the on-chip cache.

For example, a 200-MHz microprocessor whose on-chip cache has a 90 percent hit ratio will operate at only 40 percent of its potential if each miss cycle takes 80 ns or 16 clocks. But if the processor has access to a secondary off-chip cache with a 20-ns cycle time and a hit rate of 90 percent, the processor can attain 70 percent of its potential.

The two most important parameters for a secondary cache are access time and hit rate. The secondary cache hit rate must be optimized and its speed must be as great as possible.

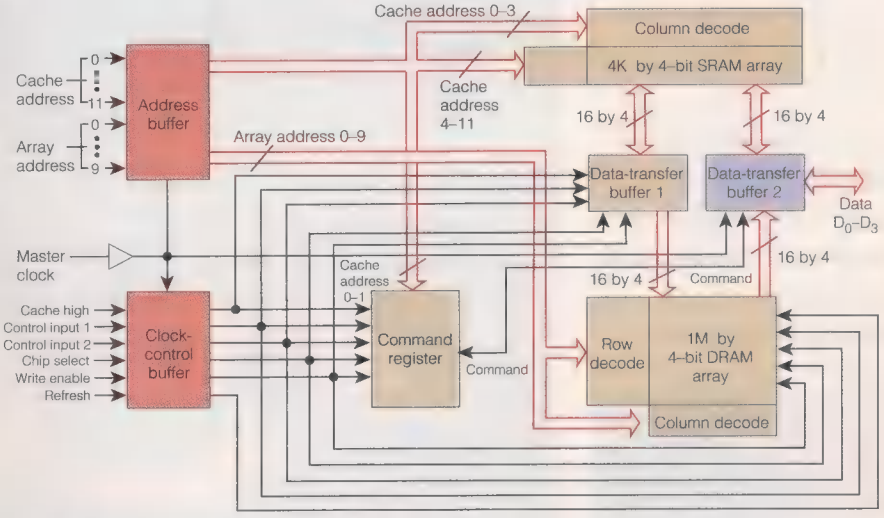
OPTIMAL HITS. A cache DRAM optimizes its hit rate by including a small static RAM and linking its static and dynamic sections by a wide data path [Fig. 3]. Depending on the benchmark, a cache DRAM improves processor utilization by 42 percent and boosts hit rate to 96.9 percent. At the same time, adding a 32K-byte static RAM cache to an 8M-byte dynamic RAM increases the die size by only 7 percent and raises the already low chip cost by only 10–20 percent.

A single bank of 4M-byte dynamic RAM on a 64-bit-wide bus can transfer data to and from a small on-chip static RAM at a rate of 1.6G bytes/s. As the number of static RAM banks is increased, data transfer rates grow even higher—eight banks transfer 12.8G bytes/s—and hit rates increase as well.

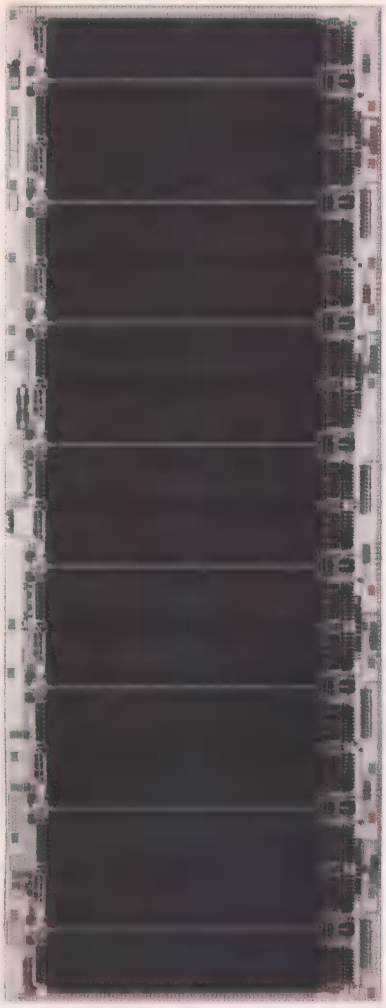
Cache DRAM does not duplicate the function of the primary cache on a processor. The primary cache usually has some associativity and a modest-size block (usually 4). A cache DRAM secondary cache usually will be direct-mapped (although associativity is allowed) and the block size will range from 16 to 64 or even larger, depending on the number of banks. Thus the primary cache works well for tight instruction loops, while the secondary cache works well as an instruction and data prefetcher. The cache DRAM secondary cache will handle context switching and data transfers very efficiently.

At least as important as the hit rate of a secondary cache is its access time. The cache DRAM architecture allows a small memory of this kind to function like a large one. Since it is easier to make a small cache fast, a 10–15-ns access time is easily achieved by the 4M-byte memory made by standard, low-cost dynamic RAM processes.

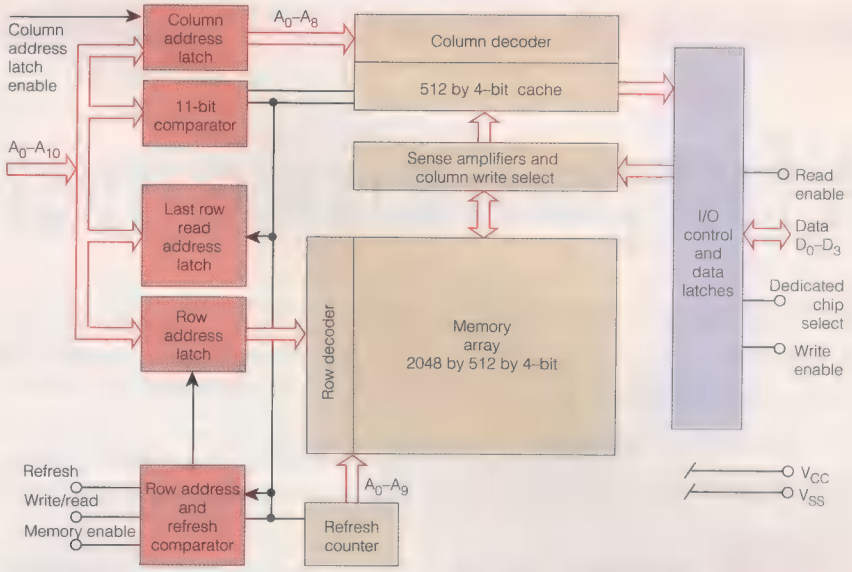
Future generations of the cache DRAM will most probably employ some type of new I/O standard (such as Gunning transceiver logic, or GTL) to further shorten the access time from processor to second-level cache. The synchronous interface that cache DRAMs now employ will probably be retained in future generations.



[3] The cache memory in a cache DRAM is a small, fast static RAM. The main memory is a standard dynamic RAM. The two memory sections communicate over a wide data path through data transfer buffers. Miss data is transferred into one buffer, while the expected data is transferred simultaneously from the dynamic RAM to the static RAM through the other buffer.



[4] An enhanced DRAM spreads static RAM cells throughout the die; they surround the light horizontal strips.



[5] In the enhanced dynamic RAM, static RAM cache directly maps to the most recent row accessed from the dynamic RAM array. This feature simplifies cache control and saves on the chip area needed for the static RAM. Data is available asynchronously and randomly from the static RAM cache at a rate of 67 MHz.

Enhanced dynamic RAM

David Bondurant
Ramtron International Corp.

When computer designers are asked what features they want in the next generation of dynamic RAMs, they will generally specify three: zero wait states on all bus cycles (not just burst reads); standard dynamic RAM (DRAM) architecture and packaging for an easy system upgrade; and no significant cost increase over standard DRAM. Enhanced DRAMs are aimed at satisfying these wants.

Having no wait states is especially important, since all waits impair microprocessor efficiency. This fact is made painfully obvious by new clock-doubled architectures where every wait state on the bus translates into two within the processor. Enlarging burst-read bandwidth without doing anything for other bus cycles solves only part of the problem. With its novel device and circuit designs, the enhanced DRAM improves performance on all bus cycles [Fig. 4].

The CMOS fabrication process for enhanced DRAMs introduces ▪ field-shield structure that actively isolates transistors in the silicon wafer and reduces their junction capacitance; the transistors switch faster as ▪ result. A 4M-bit enhanced DRAM has a row access time of 35 ns and a cycle time of 65 ns—twice as fast as most conventional DRAMs.

An enhanced DRAM chip also includes ▪ 2K-bit static RAM (SRAM) cache row register that is accessed in 15 ns. This cache provides zero-wait-state read-hit and burst-read cycles at clock rates of up to 33 MHz without interleaving and greater than 50 MHz with two-way interleaving.

DATA TRANSFER. A 256-byte-wide bus joins the 4M-bit DRAM array to the 2K-bit on-chip SRAM cache [Fig. 5]. All 2048 bits of data in the cache are updated in a single 35-ns row access, for an effective cache-fill bandwidth of 7.3 gigabytes per second. This high data transfer rate is made possible by the close coupling of the DRAM and SRAM. It reduces wait states due to read, burst-read, and multiple burst-read misses to a far lower level than is attained by employing conventional combinations of external SRAM and interleaved DRAM.

Writing data to the enhanced DRAM is speeded by an on-chip write-posting register. With it, writes may be posted to the chip in 15 ns, and then the cache may be read while the 65-ns write cycle is completed in the background. Write bursts proceed within ▪ page at 15 ns per word. This is three times faster than standard fast-page-mode DRAMs. An on-chip hit/miss comparator automatically maintains cache coherency with on-chip DRAM for write hits, without incurring ▪ speed penalty.

Since all reads occur from the cache row register, precharging is also performed in the background. The next bus cycle can start immediately without a precharge delay. Similarly, DRAM refresh can also be performed in the background of cache read operations.

An enhanced DRAM has the same address and data path ▪ a standard DRAM with page mode and static column operations from cache. An enhanced DRAM needs only five more pins than a standard DRAM—one extra address and four new control pins. It is housed in a small-outline J-lead (SOJ) plastic package, like ▪ standard DRAM.

Eight enhanced DRAMs can be combined in a single in-line memory module (SIMM) that directly replaces a standard DRAM SIMM; a computer may then be upgraded to faster memory simply by reconfiguring the memory controller. The 72-pin SIMM's capacity of 36M bits is joined to 16K bits of SRAM by ▪ 16K-bit-wide bus, resulting in an extemely high cache-fill bandwidth of 58.6 gigabytes/s.

The SRAM cache and wide bus add only ▪ little area to the enhanced DRAM chip—about 5 percent. The enhanced DRAM chip therefore costs only slightly more than a standard DRAM of equal size.

ABOUT THE AUTHORS. Fred Jones [pp. 43–48] is concept engineering manager at United Memories Inc., Colorado Springs, Colo. He previously was associate director of memory semiconductor service at Dataquest Inc., San Jose, Calif.

The authors of "Synchronous dynamic RAMs" are all with Texas Instruments Inc., Houston, Texas. Betty Prince is manager, new products, MOS Memory Worldwide Marketing. Roger Norwood is manager, DRAM design. Joe Hartigan and Wilbur C. Vogley are DRAM systems specialists.

Charles A. Hart [p. 48] is memory marketing manager at Mitsubishi Electronics America Inc., Sunnyvale, Calif.

David Bondurant [p. 49] is director of applications engineering at Ramtron International Corp., Colorado Springs, Colo. ◆

A fast path to one memory

A proprietary scheme for a unified memory system covers all design aspects to ensure fast display and quick computation

Mike Farmwald and David Mooring Rambus Inc.

The drive toward efficient yet affordable computers with high-quality graphics display has been impeded by the relative tardiness of dynamic RAMs. As a solution, engineers at Rambus Inc., Mountain View, Calif., have developed and fully specified a memory architecture that can keep up with today's fastest processors. The architecture covers devices, interfaces, buses, controllers and protocols, and is cost-effective for applications ranging from palmtops through desktop PCs to supercomputers.

The technology behind the architecture can be licensed for a royalty fee comparable to that for other patented technologies, such as traditional, video and synchronous dynamic RAMs (DRAMs). It has gained the support of three of the top five DRAM suppliers—Toshiba, Fujitsu, and NEC.

In essence, the approach reinvents the way in which memory and logic devices communicate so as to optimize performance from a system-level perspective. Standard CMOS and the existing printed-circuit board suffice to transfer blocks of data as fast as the laws of physics allow. A computer or control system built with this memory architecture need use no caches, and it improves graphics performance three- to fivefold in comparison to video RAM.

Rambus replaces extant memory types (dynamic, static, and video RAM) and their interconnects with unique DRAMs and a high-performance, chip-to-chip interface. The third special element is a high-speed channel.

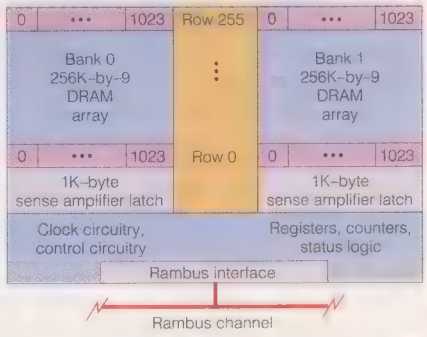
THE RAMBUS DRAM. The Rambus DRAM delivers a byte of data every 2 ns for a block of information up to 256 bytes long. Rambus allows an extra bit to be added to each byte, so a typical Rambus "byte" is usually 9 bits long. The ninth bit may be used for parity, overlays, a hardware cursor, or other functions defined by the system designer.

The Rambus DRAM utilizes the sense amplifiers and core of traditional, high-volume CMOS DRAMs. The 4.5M-bit version developed by Tokyo's Toshiba Corp. [Fig. 1] is based on a standard 512K-by-9-bit DRAM, but has two memory banks of equal size. Each memory bank has 1K byte of sense amplifier latches, accessed as if they were a cache. Because of the large size of the latches and the organization of the cache as contiguous address spaces, the hit rates to these caches are very high. Not coincidentally, mapping registers in the Rambus DRAM give flexibility in address mapping so that the locality of memory can be tailored to the application.

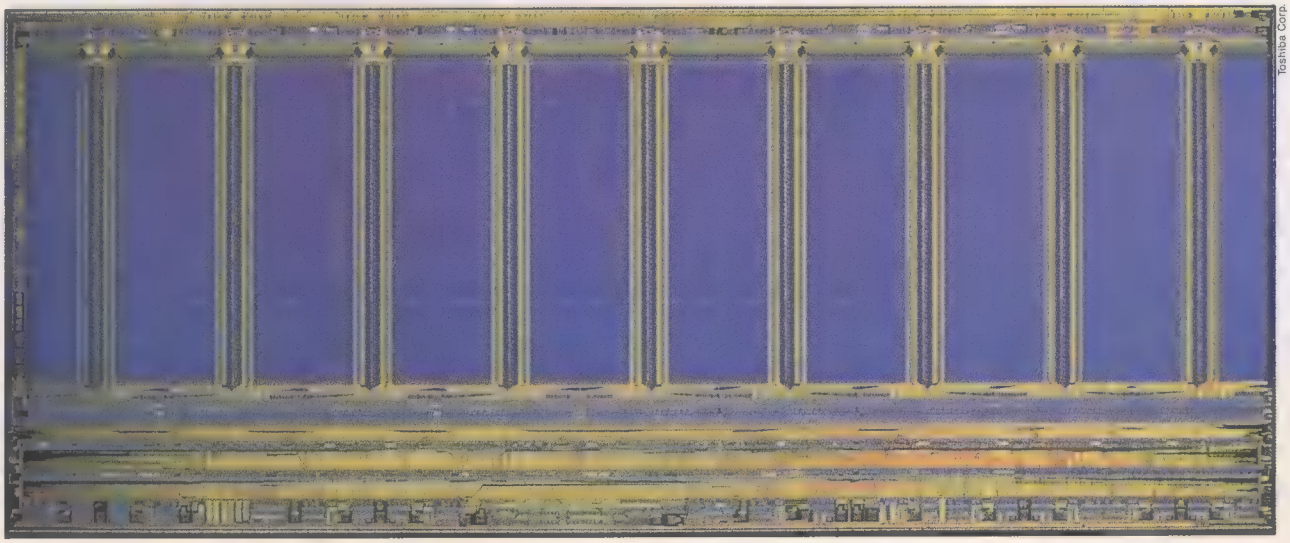
For a 4.5M-bit Rambus DRAM, the protocol overhead and the latency on a hit, together with the 512 ns it takes to transfer a 256-byte block of data, add up to only 560 ns. The miss latency, equal to the core cycle time, ranges from 150 to 200 ns. The 18M-bit Rambus DRAM has the identical pinout and works like the 4.5M-bit device, only much faster; the 68M-bit Rambus DRAM will likewise be 100 percent compatible.

The 4.5M-bit Rambus DRAM die is 14 percent larger than the traditional 512K-by-9-bit DRAM on which it is based. Larger Rambus DRAMs will come in 9- and 8-bit-wide versions, storing 18.5M and 16M bits, respectively, and able to function on the same Rambus channel. The chip overhead for 16M- and 18.5M-bit Rambus DRAMs will be even smaller because the Rambus interface is relatively fixed in size.

The interface pads are all on one edge of



[1] Along the bottom of this 512K-by-9-bit Rambus DRAM die are the Rambus interface and additional functions, including self-refresh circuitry and timing registers for response control.



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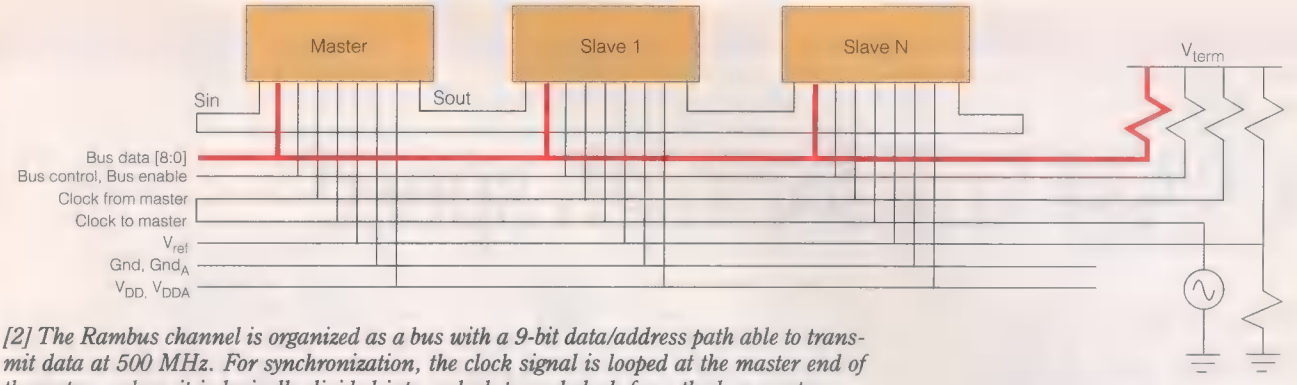

[2] The Rambus channel is organized as a bus with a 9-bit data/address path able to transmit data at 500 MHz. For synchronization, the clock signal is looped at the master end of the system, where it is logically divided into a clock to and clock from the bus master.

the die. In fact, the pad pitch matches the pin pitch, which matches the trace spacing on the Rambus channel. This provides a balanced and very light loading for every pin on the Rambus DRAM. A vertical surface-mount package contributes to a low inductance, and allows the devices to be densely packed on a printed-circuit board, adding to the memory system's cost-effectiveness. The packaging scheme has been submitted to the Electronic Industries Association of Japan and the Joint Electron Device Engineering Council for approval as a standard. The dense packaging allows a user to expand memory in increments of 1 to 32 Rambus DRAMs on a small expansion card, called the RModule.

TRANSMISSION LINE. The density of the packaging reduces the transmission distances, which helps make the Rambus channel very fast. The Rambus channel is a narrow bus only 9 bits wide that transfers address, data, and control information at 500 MHz using a synchronous, block-oriented protocol. The channel's high speed is also made possible by its high-quality transmission lines, low-voltage signal swings, and precise clocking.

The Rambus channel is a controlled-impedance transmission line environment, terminated at one end [Fig. 2]. Rambus design rules specify that all Rambus DRAMs will be on one end of the bus and a bus master that controls the memory system will be at the other end. The bus master may be any type of processor, graphics controller, memory controller, peripheral, or application-specific IC (ASIC).

The channel traces are laid out on a standard printed-circuit board with normal trace widths and dielectric thicknesses. Up to 10 sockets can lie on the channel, allowing hundreds of Rambus DRAMs to be added for memory expansion.

Transferring data on both edges of the channel's 250-MHz clock gives a maximum data rate of 500 MHz. All high-speed signals on the Rambus channel use low-voltage swings of about 600 mV; V_{ref}, a dc reference voltage of approximately 2 V, sets the logic threshold for the small-swing signals. The low-voltage swing of the signals minimizes the change in voltage (and hence current) over time, resulting in less ground bounce, less power consumption, and less electromagnetic interference. The low-voltage swings are generated by current-mode signaling—pulling current out of the bus line.

The bus is terminated at only one end, reducing power and component count. When sending data, a slave device in the middle of this bus drives half-swing signals in both directions. One signal terminates in a resistor, while the other reflects off the unterminated end, doubles in amplitude, and travels back to the terminator.

Two features make single-end termination workable: the high impedance of the output drivers, and the location of the bus master. First, the output drivers' high impedance eliminates the wired-OR glitch seen with emitter-coupled logic (ECL) technology. The lack of wired-OR glitching allows superposition of the current-mode signals without the mutual interference of clipping found in voltage-mode signaling.

Second, the bus master is either the source or the destination of all data packets. The master, located at the open, or unterminated, end of the bus, drives full-amplitude signals to all the slaves. On the other hand, when a slave drives the bus with half-swing signals, the master receives it "reflected" to full amplitude.

To eliminate clock skews, clock and data signals are made to travel in the same direction in a Rambus system. The clock begins at the slave end of the channel, labeled at this point as clock to master, and propagates to the master end. There, it loops back, as clock from master, to the slave end, where it terminates. A slave sends data to the master synchronously with clock to master; the master sends data to the slaves synchronously with clock from master. Matched transmission lines ensure that clock and data are synchronized as they propagate to their destination.

DEVICE INTERFACE. To attach to this channel, devices must have a special interface. A detailed specification covers electrical, logical, and mechanical connections and makes a simple cookbook process out of the design of an ultrahigh-speed chip interface using standard submicrometer CMOS processes. Along with state-machine design techniques, the specification ensures that all Rambus devices are 100 percent compatible, whether they are off-the-shelf components or a cell in an ASIC library.

Having a central processing unit (CPU) with a built-in Rambus interface increases overall system performance. It is also possible, however, to connect a standard CPU to a Rambus I/O controller over the CPU's standard bus. Thus any standard CPU may be used, and it can run at a higher clock rate because of the light loading on its bus.

Since all Rambus interface implementations are functionally identical, a design engineer is free to interface any controller to the Rambus channel without concern for the specific implementation of the interface cell itself.

The interface consists of serial-to-parallel and parallel-to-serial converters plus clock-recovery circuitry. The interface converts the Rambus-channel data rate of 1 byte every 2 ns to 8 bytes every 16 ns, and it raises the small-voltage swings used on the channel to CMOS levels.

The application designer implements the logical layer of the Rambus protocol. Sample protocol-logic designs from Rambus Inc. serve as a guide.

ANOTHER WAY. Rambus technology provides an alternative solution for many design problems. For instance, an i486 system with Rambus controller and Rambus DRAMs performs on a par with a system having a second-level cache.

The 500-Mbyte/s bandwidth of the Rambus channel is well suited to two- and three-dimensional graphics and 24-bit, true-color displays. For a 128-byte bit-aligned block transfer, the Rambus DRAM averages 2.1 ns per byte, compared to 12 ns per byte for a 32-bit-wide video RAM solution.

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A RAM link for high speed

Work on a new, open standard that defines a ring for linking fast memories and processors is well under way

To maximize memory system throughput yet keep latency low: that is just one of the primary goals of a new high-speed RAM interface being developed for standardization. Another goal is to minimize the number of devices required for small, high-performance multiprocessor systems.

Coupling these goals in the design of the new interface, called RamLink, requires some unique structuring. Because the hit rate for caches is likely to be low in multiprocessor environments, RamLink must provide high performance even when dynamic RAMs (DRAMs) having internal caching mechanisms are ineffective. In addition to RAM, RamLink will support flash nonvolatile memory, read-only memory, and even memory-mapped disks (Computer Society Project P1285).

At present, the P1596.4 working group developing the interface seems to have converged on its basic design model. Performance modeling and evaluation is nearing completion and work on detailing the control and status register configuration has started. The project was begun in 1991 by Hans Wiggers of Hewlett-Packard Co., Palo Alto, Calif., to solve some of the problems of present-day RAMs by applying technologies developed for the Scalable Coherent Interface (SCI).

The SCI (IEEE Std. 1596-1992) is intended to replace computer buses in the next generation of computers, from high-end multiprocessors to workstations or even PCs. To provide bus-like services without the disadvantages of bused connections, the SCI uses unidirectional, point-to-point differential links at gigabyte-per-second speeds with a packet-based protocol. Since this signaling mechanism has great potential for higher speed as technology evolves, the RamLink project seeks to specify signals and links suitable for the next generation of SCI ICs [see pp. 54–57].

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MISMATCHING PROBLEMS. While designing systems using the SCI, engineers observed that present memory devices are poorly matched to high-performance entry-level workstations or high-definition television (HDTV) systems. The low bandwidth at the I/O pins of the DRAM forces designers to use a wide DRAM array. For even higher bandwidth, several of these wide arrays must be interleaved.

Such a design results in a large number of chips for even the smallest high-performance system, unreasonably big memory and high cost for the entry-level product, and excessive upgrade increments. This mismatch gets worse as DRAM capacity increases, and is already a practical problem.

After exploring a variety of connection topologies, including some that used bus-style connections, the group concluded that the most attractive possibility was using low-voltage differential-signal (LVDS) links to connect memory chips in small rings [Fig. 1]. A dedicated controller communicates with each memory chip in the ring by sending packets over the link. It also schedules all ring activities and interfaces the ring to the SCI, a processor bus, or some other system bus.

> An access scheme must provide high performance even when DRAMs with internal caches are ineffective

RamLink uses a much simplified version of the SCI's protocols. Since RamLink uses only one controller per ring, it can handle contention for resources and scheduling of ring bandwidth. This treatment not only shortens the packets, thereby reducing latency, but also simplifies and speeds the RAM chip interface.

RamLink's high bandwidth is a good match with both the already high internal bandwidth of row accesses and the performance and packaging needs of the next generation. It can run its links at 500 megabytes per second with existing high-performance technology, using uncomplicated layout, packaging, and connectors; bus-style connections have inherent turnaround delays and loading problems that require optimization of physical layout and packaging to reach a comparable speed. Ramlink's speed may also increase as technology advances in the future.

A breakthrough that will simplify RamLink chips is an encoding and scheduling method that eliminates the need for a chip to examine a packet before passing it along. Using this scheme, an incoming packet is passed from input to output as fast as possible. It typically goes through only one register, whose main purpose is to remove any accumulated skew between the parallel link signals. The chip copies the packet internally, decoding it at its leisure, and discarding or acting on it as appropriate.

Thus the delay through each RamLink chip is only about 1 bit-time or, in the first generation, 2 ns. Even this delay may possibly be reduced using flow-through techniques, that is, selectively disabling the deskewing latches on many of the chips.

COLLISION AVOIDANCE. A RamLink controller schedules all packet activity to avoid collisions. The header of any memory request packet it sends contains a field that specifies when a response should be sent, given either as a precise time or as an upper bound. When a RAM transmits, it blindly discards anything coming in while emitting its packet on its output link. This encoding makes packet boundaries unambiguous, so the controller will not be confused by partly overwritten packets.

If the RAM cannot return the requested data on schedule, it sends instead a packet with appropriate status bits so the controller knows it should try again later. This might occur if the RAM is the cache for a P1285 memory-mapped disk drive and the access is a cache miss; a simple "service-required" signal can be used to alert the controller when the disk is ready to service the retried request.

MULTIPLE BANKS. So that requests can be overlapped in order to increase the throughput while keeping latency low, it is critical to have multiple memory banks for high-performance systems. In the RamLink architecture, each RAM chip is at least one memory bank, and it may be several (queuing and processing multiple requests inter-

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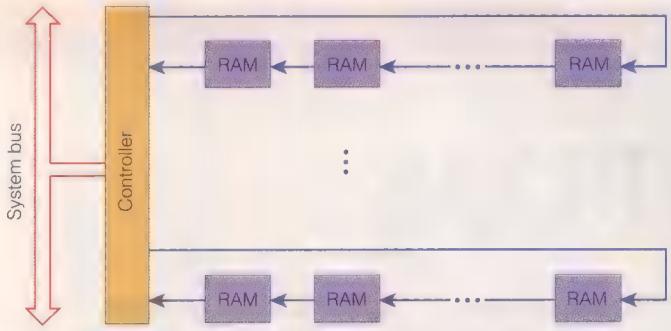
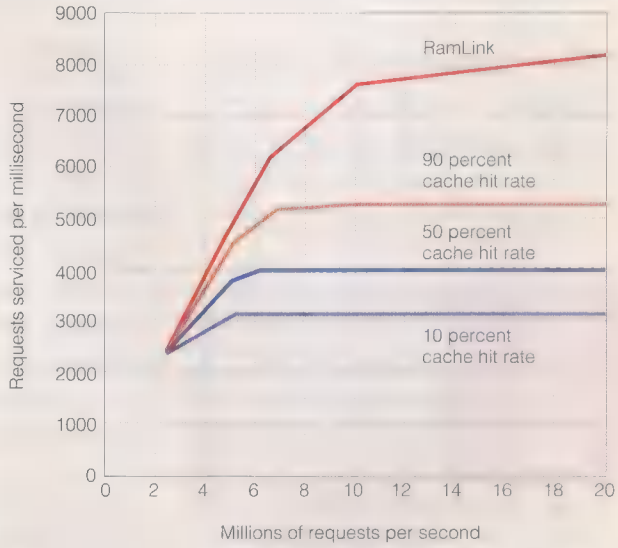


[1] RamLink is the architecture being proposed by the IEEE Computer Society's P1596.4 working group for next-generation computer systems. It uses a ring topology, rather than a bus, to reduce round-trip travel time (turn-around delays) and loading problems. In its initial version, the ring can support a 500-MHz transmission rate, transferring a byte every 2 ns. The ring's byte-wide protocol for transferring information accepts packets of up to 64 data bytes, reducing the overhead of the 6-byte header and 2-byte tail.



[2] The performance of both a RamLink ring using memory chips without internal cache was simulated, as was that of a Rambus system using internal-cache memories with 90-, 50-, or 10-percent cache hit rates. The results indicate saturation behavior and the limits on throughput under these conditions.

nally). Of course, for still higher throughput and capacity, more RamLink rings and controllers can be added as desired.

It seems likely that RAM functionality will increase with time, so the RamLink control protocols are designed to expand easily. Two request-packet formats are defined: one with 32 bits for the internal byte address within a RAM chip and one with 48 bits. The larger format should not be needed for some time; the first likely application would be for memory-mapped disk drives. RamLink defines a variety of transfer lengths, from a single byte to an entire cache line.

Those who need redundancy may use parallel RamLink rings to make a wide path with correcting codes, so that failure of any one ring will not stop the system, much as with redundant arrays of disks. RamLink defines an optional 9th bit in the data path, to be used for error-correcting codes or parity data. There is also provision for scheduling refresh operations and for self-refresh.

SIMULA SIMULATION. A detailed simulation model for RamLink has been written in Simula, an object-oriented language. It uses the graphics capabilities of the X11 interface, so it is possible to watch how packets are transported between the controller and the RamLink memory chips. The graphic interface was particularly valuable not only for understanding various scheduling algorithms but for debugging the simulation program, too.

For simplicity, the initial simulations assumed a random and independent arrival of read and write requests. The requests are drawn according to a negative-exponential distribution, and read and write requests are equally likely. All read and write requests were for a full cache line of 64 bytes, but the simulation did not take memory-refresh delays into account.

The model of a memory controller used for the simulation had a four-slot input queue for new memory requests; two queue slots were for read requests and two for write requests. If the queue was full, the request was not serviced and was counted as a "turned down" request in the simulations. Latency was calculated from the moment the request was put into the queue until the time the first data byte of the RAM's response arrived at the controller.

The projected performance of RamLink was compared to Rambus, an emerging commercial architecture that uses the same signaling speed but a bus-style connection. Rambus DRAM employs its internal row buffer as a "cache," which speeds subsequent reads from nearby addresses. The latency for a Rambus DRAM read request is 48 ns for a cache hit, 208 ns for a miss. RamLink's simulations used a 16-chip ring with a transport delay of 2 ns per chip. The latency of a RamLink read request is 128 ns. All latencies are for the best case, namely, only one outstanding request.

Rambus DRAM behavior is simulated for three different "cache" hit rates—10, 50, and 90 percent—because the hit rate has a big effect on performance. A 90 percent hit rate is conceivable in a uniprocessor system, but the lower hit rates are more likely in a multitasking or multiprocessor system. RamLink was not simulated using RAM chips with internal cache, as hit rates will be low for a multiprocessor environment.

The behavior of RamLink and Rambus DRAM was also simulated under different system loads: a lightly loaded system having a mean arrival rate of 2.5 MHz for memory requests (a request is a read or write of 64 bytes of data), and a heavily loaded system, most likely a multiprocessor system, having a mean arrival rate of 10 MHz. Figure 2 plots the requests serviced in a simulated millisecond against the rate of requests presented to the controller.

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Fast interfaces for DRAMs

The fundamental circuitry between a device's interior logic and its external pins must evolve to meet new speed and power needs

If dynamic RAMs and processors are to trade data at close to top speed, the interface between them must be re-engineered. At a minimum, it must support speeds in the 100–500-MHz range, the low end for new dynamic RAM architectures and the high end for the speed projected for processors by the decade's end.

None of the types of interfaces now popular can do this while conserving power and cost to the desired degree. Yet it is hardly prudent to move on to a new form of interfaces without learning from and allowing for what has gone before.

TODAY'S LIMITS. Current nominal 5-V interfaces include standard CMOS and TTL. CMOS is usually specified as having a minimum (worst-case) 2-V swing, but (unless dc-loaded for some special application) usually goes rail to rail at 5 V. On the other hand, TTL is typically specified as having a 2-V swing because it does not go rail to rail; the dc load of its fanout and its emitter-follower pull-ups prevent this from occurring. Even so, TTL typically achieves much more than a 2-V swing and, with a 5.5-V maximum V_{CC} (worst case), it may well operate at almost twice the 2-V level. Low-voltage CMOS and TTL are emerging; the nominal 3.3-V LVCMOS goes rail to rail to about a 3.6-V (worst-case) output swing, while LVTTL retains the 2-V output swing of its more power-hungry predecessor [see table, p. 56].

Regardless of whether it is pumping lumped-capacitance loads or driving terminated lines, a rail-to-rail swing consumes too much power. The tracks on the typical printed-circuit board look like 100-Ω lines, but lumped-capacitance point loads in a bus environment can complicate things, lowering this figure to an effective characteristic impedance (Z_o) well below 50 Ω [Fig. 1].

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At 100 MHz, each output driver must dissipate over 100 mW to drive a 100-pF lumped load rail to rail with 3.3-V supplies. Each 100-MHz DRAM could have as many as 16 output drivers operating simultaneously, collectively dissipating over 1.6 W. Not surprisingly, the fine print on data sheets for such parts commonly notes that "power consumption is specified with no load." Transition times for 100-MHz signals are necessarily around 2 ns while, for a track distance of 15 cm on a printed-circuit board, transmission time is typically 1 ns. If proper termination is not used, reflections will harm signal integrity under such circumstances.

For many years, emitter-coupled logic (ECL) has been the usual choice for high-speed interfaces. The limited swing of ECL signals and ECL's ability to drive terminated lines made it superior in high-speed systems to the ubiquitous TTL interface.

TTL, however, is relatively easy to implement in either MOS field-effect or bipolar transistor technology, whereas ECL interface specifications revolve around the technology of bipolar transistors. And attempts to match ECL with FET devices have, to date, had little success.

Bipolar CMOS (BiCMOS) technology can overcome this ECL drawback, of course. But whether BiCMOS will be applicable to all future high-speed devices is debatable; the present economics of adding bipolar capability to all MOS chips just for the output drivers casts doubt on its future.

> In practice, it is difficult to define an interface standard in a way that ensures wide acceptance

NEW PATHS. Because of all these limitations, new proposals are being put forward for achieving ECL's low swing and ability to drive terminated lines with optimized MOS circuits. Common to all the interfaces proposed here—center-tap terminated, Gunning transceiver logic, and low-voltage differential signaling—is a restricted signal swing, on the order of 1 V or less; however, the base levels from which the swing takes place vary widely.

In practical terms, it is difficult to define a standard interface in a way that ensures wide acceptance. It is not sufficient that adherence to a standard may result in a working system under ideal conditions; a standard must be based on a realistic means of testing for and specifying worst-case performance. Only then can a component that meets the specification be guaranteed to perform under realistic system conditions.

Components with present-day interfaces are already running into test and specification problems. A chip with restricted-swing interfaces is very difficult to test to worst-case specifications. Nor is agreement easy as to what constitutes a realistic environment.

Various new approaches for specifying electric interface characteristics are being considered, such as supplying a set of simulation parameters for a circuit's output drivers. This is a radical departure from the traditional component data sheet, and no one yet fully understands how to test an actual product to ensure that its parameters match those of the simulation.

Center-tap terminated interface

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Like low-voltage CMOS, which has adopted logic levels that reflect 30-year-old TTL standards, the center-tap terminated interface is an evolutionary, back-compatible standard that will ease the transition to new speed requirements.

When used unterminated in short-run situations, center-tap terminated (CTT) drivers give regular rail-to-rail swings and CTT receivers have standard input threshold levels. But for longer runs where termination is essential, CTT drivers automatically adjust to a restricted swing with a termination voltage near mid-level. The logic swing is set to a minimum of ±400 mV relative to the termination voltage. The same level is used as an external reference input to CTT receivers, allowing tighter control of input levels than with simple CMOS input buffers.

None of the circuit elements needed for CTT are really new. Input buffers using internal reference levels have been widely used in dynamic RAMs (DRAMs). Supplying the reference level externally allows the

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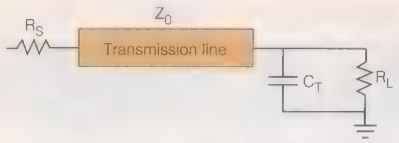

[1] At high speeds, traces on printed-circuit boards become transmission lines with characteristic impedance Z_0, which is dependent on the line's inductance and capacitance per unit length. If these lines are buses, instead of simple point-to-point connections, Z_0 is reduced to Z' by the connected loads. (These loads, typically capacitive, are shown here for convenience as a single load capacitance, C_T, but actually spread along the transmission line.) The size of the reduction in Z_0 is based on the ratio of line to load capacitance. When line termination R_L matches Z', there are no reflections and the signal is transmitted cleanly. But if R_L is not equal to Z', reflections will distort the signal.

minimum high-input level and maximum low-input level (the worst-case input levels) to be tightened from 2.0 and 0.8 V, respectively, to ±200 mV, while maintaining acceptable margins for design differences and testing requirements. Standard CMOS output buffers in high-speed static RAMs (SRAMs) are routinely tested with terminated lines, and the control of output swing by feedback techniques has many precedents.

One circuit implementation uses a digital form of feedback for preventing excessive swing when driving terminated loads [Fig. 2]. The driver's output state is monitored by an input receiver, which also serves as an input buffer when the terminus is an I/O port. While the output is opposite to the desired state, additional output drive is provided, so performance can match regular LVCMOS when driving large, lumped-capacitance loads. Once the output is in the desired state, the drive is cut back so that there will be limited swing if a termination resistance is present. Latches ensure that any reflection forcing output levels back toward the original state cannot re-trip the more powerful drivers.

While back compatibility forces some compromises—in this case, slightly higher power dissipation in the drivers relative to an open-drain asymmetric driver—benefits include lower system power from symmetrical drives. In the long term, systems employing CTT may evolve to use equal plus and minus supplies relative to a ground reference plane, with signals symmetrically disposed.

Gunning transceiver logic

Richard Rodgers
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Systems will fully utilize the computing power of present-day very large-scale integration only if IC interfaces change radically. The electric noise created by the nearly rail-to-rail swings of 5-V TTL is far too great and drags out settling times far too long. Even the adoption of low-voltage devices with output swings near 3 V will do little to help the arrival of the transmission speeds users demand for system performance. What is needed is the speed and performance of emitter-coupled logic or bipolar CMOS (ECL and BiCMOS), but at the power and cost of TTL-compatible CMOS.

Gunning transceiver logic (GTL) implemented in CMOS easily meets these needs. Additionally, since its output voltage level is independent of V_{CC}, GTL can be a force for stabilizing the interface environment device voltages are reduced below the 5-V level.

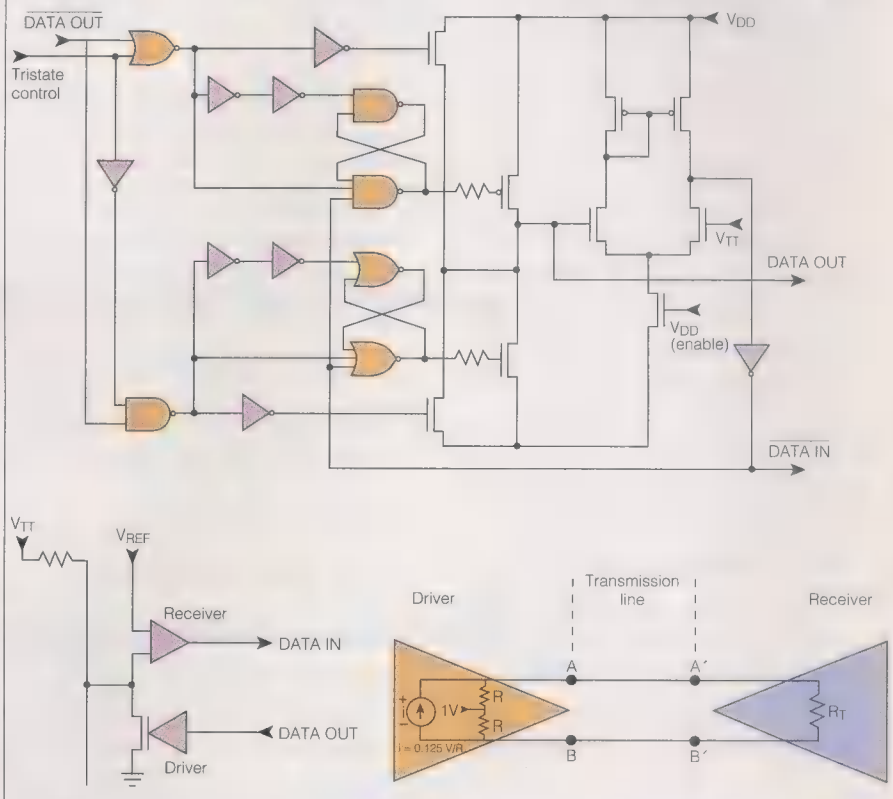
Unlike the current-driver interfaces being proposed, for which the output voltage can change dramatically as the output load changes, GTL output voltage levels are essentially the same, both for terminated and unterminated applications. As a single-ended scheme, it does not require two wires for each connection and hence does not increase the pin requirements for each device, as differential interfaces do. Nor is GTL simply a specification in process or a preliminary design; thousands of devices have already been fabricated and boards using GTL are currently being used in a system prototype.

The logic's I/O interface lets CMOS devices communicate at very high speed over terminated transmission-line paths. GTL will also enable processors, application-specific ICs (ASICs), and synchronous memories to operate at 100 MHz with conventional clocking. With reduced clock skew and better data synchronization, 400 MHz and higher data rates could be reached.

At 0.8 V (nominal), GTL's signal swing is comparable to that of ECL. Because of this similarity, most design tools and practices developed in the last 20 years for building top-performance ECL systems are applicable to GTL interface design.

The low signal-voltage levels keep on-chip power low. Whereas an ECL output typically uses about 125 mW, a similar GTL circuit consumes only 10 mW, so it is practical to include hundreds of GTL I/O circuits on one ASIC.

A simple way of seeing the power impact of Gunning transceiver logic is to compare the power requirements for high-speed devices with 160 active I/O drivers that use different types of logic levels: emitter-coupled logic (ECL), backplane transceiver logic (BTL—a form of high-speed inter-



[2] Three techniques have been suggested for high-speed interfaces: center-tap terminated (CTT), Gunning transceiver logic (GTL), and low-voltage differential signaling (LVDS). The CTT driver [top] can handle both standard and reduced signal levels; the termination voltage, V_{TT}, controls the levels of the logic swing, which can be as high as 5 V. In a GTL interface [bottom left], when the n-channel driver is turned off, it is pulled up to the V_{TT} level (nominally 1.2 V) by an external resistor; the receiver differentially compares an incoming signal to V_{REF}, typically 0.8 V. The GTL signal range is 800 mV. LVDS is unique in that it uses paired signal paths; differential signaling makes LVDS's low-amplitude (400-mV) signals insensitive to noise, but doubles I/O pin count.

face developed by National Semiconductor Corp. in the late 1980s and now in the public domain), and GTL. If implemented with ECL, the drivers would consume 20 W with ■ 50-Ω, 3.0-V termination at both ends. If the drivers were implemented using BTL, then they would require a power budget of 11 W with a 50-Ω, 2.0-V termination. For the same number of drivers, however, GTL would draw only 1.5 W with 50-Ω, 1.2-V terminations, suiting battery-powered portable devices that require high performance.

GTL's low output-stage power allows devices to drive a local motherboard bus directly, without external drivers, thereby lowering cost and simplifying the interconnect. The device cost is low, since current CMOS technology is sufficient; BiCMOS could be used, but is not required. Further, GTL designs can be used without modification as the chip's V_{DD} level is reduced with new CMOS process developments; GTL parts designed for ■ V_{DD} of 5 V can readily communicate with those designed for 3.3 V or less. The effect will be to stabilize the industry, as V_{DD} might be lowered more than once in the next decade.

Second-generation GTL CMOS I/O transceivers are currently being used for both backplane and motherboard interchip bus signals in a high-performance computer system intended for volume production. This includes ASICs with up to 160 GTL I/O cells operating at data rates greater than 100 MHz. Many companies are currently investigating or developing GTL devices, and Xerox Corp. has proposed GTL for industry standardization. At present, the technology may be licensed for ■ nominal fee.

A GTL output driver typically uses an open-drain n-channel device, which, when turned off, is pulled up by an external terminating resistor to the terminating voltage, V_{TT}, which is equal to 1.2 V. A GTL input receiver is a differential comparator with one side connected to the reference voltage, V_{REF}, which is typically 0.8 V.

Alternatively, an active pull-up GTL output driver may be used for short signal paths with no external terminating resistor. For an upper-level return for the pull-up transistor, V_{TT} is brought to a device pin so that the 1.2-V upper level is maintained. Figure 2 shows ■ bidirectional transmission line built using GTL I/O transceiver cells.

Characteristic voltage levels for commonly used logic

	Power supply voltage, volts	Minimum high output, volts	Maximum low output, volts	Output swing, volts
TTL	5	2.4	0.4	2
Low-voltage TTL	3.3	2.4	0.4	2
CMOS	5	$V_{CC} - \Delta$[1]	Δ	V_{CC} (5 max)
Low-voltage CMOS	3.3	$V_{CC} - \Delta$	Δ	V_{CC} (3.3 max)
Emitter-coupled logic (10K)	−5.2	−0.9	−1.2	0.3

1 Δ = voltage drop due to internal drive requirements.

Low-voltage differential signaling

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Low-voltage differential signaling, or LVDS, is the current focus of the IEEE Computer Society P1596.3 working group now developing a high-speed signal interface. The group is seeking an alternative to the ECL-level signals specified by the IEEE Std 1596-1992 Scalable Coherent Interface (SCI). The P1596.3 work is nearing completion. Some additional circuit prototyping and simulation is planned, and some questions remain on how to specify certain parameters.

The group's goal is to specify ■ new interface that will perform at least as well as emitter-coupled logic (ECL) but cost less for CMOS implementations. It is becoming increasingly clear that fast signals must have small amplitudes to keep power consumption to ■ level that can realistically and cost-effectively be handled by devices. Also, the variety of technologies likely to be used in the next few years should be capable of generating and receiving small-amplitude signals.

Most logic signals in use today are single-ended. They propagate on ■ single conductor to ■ receiver, where their voltage level is compared to an easily distributed voltage standard (often the ground, but sometimes another reference).

But these signals co-exist with noise from many sources. If they are too small, communication becomes unreliable because of noise on the signal conductor or on the reference voltage standard. Practically, the limit for single-ended transmission is a little less than 1 V.

> Fast signals need small amplitudes to keep power consumption to a satisfactory level

For really high speeds and/or really low power, however, much smaller voltage swings are desirable. To eliminate the noise problems, the wiring is arranged so that the reference voltage is exposed to the same noise as the signal. Thus, the reference is generated near the signal driver, follows the same path (twisted pair or coaxial cable), and is compared to the signal at the receiver. It is even better to transmit the signal complement instead of a constant reference so the receiver merely determines which of the two is more positive. A shield on the cable may further improve noise immunity [Fig. 2, bottom right].

At very high speeds, the advantages of this differential signaling become even more significant. The receiver is designed to ignore any voltage that appears equally on the two conductors (common-mode rejection). In high-speed systems of any real size, high-frequency noise makes the concept of a system-wide ground or any other distributed reference ■ fiction. Noise problems of this sort have been endemic for years, and are often described as ground bounce. The usual solution is to slow the system with low-pass filtering and "settling" delays until it works.

It is important to use ■ differential signaling method that maintains a constant net current flow. The net signaling current usually flows back from the receiver termination to the transmitter through the ground, so any high-frequency variations in that current contribute to system noise.

Even if the net current is constant, reversing the direction of the link (by turning drivers off at one end and on at the other) alters the sign of that current, causing noise. Thus for good system design the net current should be zero, or the links should neither be reversed nor turned on and off. (IEEE Std 1596-1992 Scalable Coherent Interface—known as SCI—mandates differential ECL signaling, with the termination current returned through the cable or cable shield. It also runs the links continuously and in one direction.)

Reversing links, in fact, is incompatible with SCI's scalability. Even if the net current is zero, the reversal introduces a sensitivity to physical scale, because the time required for reversal varies with cable length.

The smaller the signal, the easier it is to drive and the more difficult it is to receive. Thus a balance must be sought between these conflicting requirements, and the appropriate one depends on the technology considered. The LVDS working group has chosen a signal peak-to-peak amplitude of 0.25 V (minimum) at the driver, centered on +1.0 V relative to ground. Receivers should accept signals between 0 V and +2.0 V, thus allowing for up to 1 V of common-mode noise or ground shift.

This compromise seems compatible with a variety of technologies, and so the standard should be useful for some time. Differential signaling can double the I/O pin count (though this is partially offset by a reduction in the number of ground pins needed). Further, the higher speed capability lets engineers design with data paths that are narrower than would be possible with other, slower schemes, which also reduces the number of pins that would be needed.

There are additional refinements. For example, the driver impedance is constrained to be reasonably constant, independent of the logic state; then common-mode noise that propagates backward and reflects off the drivers is not converted into differential noise by different reflection coefficients on the true and complement signal lines. The receivers have on-chip differential termination resistors, possibly active devices that are servo-matched to an external reference (which relaxes the IC fabrication tolerances).

LVDS receivers can be designed to accept larger common-mode voltages (at some increase in cost). However, environments that need more than 1 V often need to handle many volts, requiring optical or magnetic isolation instead.

P1596.3 is also defining the encodings for 4-bit- and 8-bit-parallel LVDS links suitable for SCI. The first applications for the LVDS signals are a CMOS implementation of SCI, using 1-byte-wide links at 500 Mbytes per second, and RamLink [P1596.4, described on pp. 52–53.]

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To probe further

Computer Architecture: A Quantitative Approach by John Hennessy and David Patterson (Morgan Kaufmann, San Mateo, Calif., 1990) contains an excellent chapter on memory hierarchy, as does *High-Performance Computer Architecture* by Harold S. Stone (second edition, Addison-Wesley, Reading, Mass., 1990). *Computation Structures* by Stephen A. Ward and Robert H. Halstead Jr. (MIT Press, Cambridge, Mass., and McGraw-Hill, New York, 1990) discusses the impact of memory structures on design and performance for a wide range of computer architectures.

A table in the article "How DEC developed Alpha" [*Spectrum*, July 1992, pp. 26–31] provides performance ratings for high-speed processors and serves as an indicator of the type of performance required for high-level workstations. It also indicates how cache is used internally in the design of modern reduced-instruction-set processor chips. Each year, in its April issue, *Spectrum* surveys the latest developments in personal computers and workstations in a special focus report, including system performance and memory available to support such systems. The use of memory in supercomputers was covered in the September issue of *Spectrum*.

HDTV: Advanced Television for the 1990s by K. Blair Benson and Donald G. Fink (Intertext Publications, New York, and McGraw-Hill, New York, 1991) is a source of basic technical information on high-definition television. An overview of international developments in HDTV appeared in "Chasing Japan in the HDTV Race," [*IEEE Spectrum*, October 1989, pp. 26–30] and is one of the technologies that will be reviewed in the January 1993 issue of *Spectrum*. A detailed technical discussion of one of the advanced television features—ghost canceling—that will affect memory requirements appeared in "Good-bye to TV ghosts" in last July's *Spectrum* [pp. 50–52].

Semiconductor Memories by Betty Prince (second edition, John Wiley & Sons Ltd., Chichester, England, 1991) provides a global view of memory chip technologies, including detailed discussions of the internal organization of static and dynamic RAMs, as well as such other solid-state memory technologies as video RAMs, field-alterable ROMs, and flash memories. For anyone interested in semiconductor memories, it is the basic text.

Standardization efforts on synchronous dynamic RAMs were first reported by Ron Wilson in "Jedec hustling to spec new SDRAM" in the March issue of the *Electronic Engineering Times*, p. 1. The best direct source of information about the status of standards for synchronous DRAMs is the Joint Electron Device Engineering Council (Jedec), 200 Pennsylvania Ave., N.W., Washington, D.C. 20006; 202-457-4973. Jedec has taken to issuing periodic updates on the status of standards activities in committees JC-43 and JC-16, despite a long-standing policy of not allowing discussions of ongoing standards activities. When they become available, Jedec standards may be obtained from Global Engineering Documents, 2805 McGaw Ave., Box 19539, Irvine, Calif. 92713-9539; 800-854-7179.

New DRAM technologies are discussed each year at the IEEE-sponsored International Solid State Circuits Conference (ISSCC). This year's conference included a special evening discussion session on how ultralarge-scale integration (ULSI) would affect dynamic RAM, in addition to a regular daytime session in which new DRAM technologies were discussed. Copies of the proceedings may be obtained from the IEEE Service Center Single Publication Sales Unit, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331. Next year, the conference will be held from Feb. 24 to 26 at the San Francisco Marriott Hotel. For further information, contact Diane Suiters, c/o Courtesy Associates, 655 15th St., N.W., Suite #300, Washington, D.C. 20005; 202-639-4255.

Digital Bus Handbook, edited by Joseph Di Giacomo (McGraw-Hill, New York, 1990), contains chapters that discuss topics such as transmission lines, crosstalk, and transceiver technology, as well as other bus-related issues that are very applicable to memory systems. Some basic information on high-speed transceiver logic can be found on pp. 191–196 of Prince's previously cited book, *Semiconductor Memories*. Also, the IEEE *Journal of Solid State Circuits* often publishes articles related to this topic, and discussions can often be found in articles concerning dynamic RAM design.

The use of lower working voltages for ICs, which has a heavy impact on interface technologies, was the focus of the article, "ICs going on a 3-V diet," by Betty Prince and Roelof H.W. Salters in the May 1992 issue of *Spectrum*, pp. 22–25. Jedec Standards 8.0 and 8.1, which specify 3-V IC requirements, may be obtained from Global Engineering Documents at the address previously provided.

ACKNOWLEDGMENTS. The editors would like thank all of the contributing authors, but especially Betty Prince of Texas Instruments Inc., Houston, Texas, for her help in conceptualizing and organizing this series, as well as in expediting the creation of the articles it contains.

In addition, the editors would like to thank the panel of reviewers. Members of that panel included: Harvey C. Nathanson, Westinghouse Science & Technology Center, Pittsburgh; W. David Pricer, IBM Corp., Essex Junction, Vt.; Howard Sussman, NEC Electronics Inc., Natick, Mass.; and Lu Tran, Micron Semiconductor Corp., Boise, Idaho.

Fuzzy fundamentals

This orderly design procedure can save time and help prevent problems in the development of fuzzy logic systems

Fuzzy logic has rapidly become one of the most successful of today's technologies for developing sophisticated control systems. With its aid, complex requirements may be implemented in amazingly simple, easily maintained, and inexpensive controllers. The same fuzzy technology, in the form of approximate reasoning, is also resurfacing in information technology, where it provides decision-support and expert systems with powerful reasoning capabilities bound by a minimum of rules.

Of course, fuzzy logic is not the best approach for every control problem. As designers look at its power and expressiveness, they must decide where to apply it, and also how best to manage software projects based on this new technology. Increasingly, project managers, system architects, and design engineers are asking the tough questions: what types of projects can benefit from the use of fuzzy logic? How do I control projects with this technology? What is the best way to design, develop, deliver, and test systems using fuzzy logic and its related technologies?

FIT TO BE FUZZY. Fuzzy logic is a method of easily representing analog processes on a digital computer. These processes are concerned with continuous phenomena that are not easily broken down into discrete segments, and the concepts involved are difficult to model—sometimes extraordinarily so—along mathematical or rule-based lines.

An example might be an anti-lock braking system for an automobile. The control rules for a system of this nature might include such variables as the car's speed, the brake pressure, the brake temperature, the interval between applications of the brakes, and the angle of the car's lateral motion relative to its forward motion. These variables are all continuous, and the range of their values subject to interpretation by the system designer.

Thus the variable "temperature" might have a range of states: cold, cool, moderate, warm, hot, very hot. Yet the change from one state to another is not precisely defined. At no point can an increase of a tenth of a degree be said to change "this is warm" into "this is hot." Consequently, the idea of what is cold, what is warm, and what is hot is subject to different interpretations by different experts at different points in the variable's domain.

This subjectivity has profound implications for continuous system modeling, and is at the heart of the power and flexibility of fuzzy logic. With fuzzy logic, control statements are written in terms of these imprecise ideas of what constitutes the states of the variable. As an example, a fuzzy rule in an anti-lock braking system might be:

►*If brake temperature is* **Warm** *AND speed is* **Not very fast**, *then brake pressure is* **Slightly decreased**,

while a rule in a conventional proportional-integral-derivative (PID) controller would need to be very specific:

►*If brake temperature is greater than 280 AND speed is less than 45, then brake pressure is 190.*

Not only is the fuzzy logic rule more natural, and technically more expressive, but it will fire over a wider range of brake temperatures and car speeds. The degree to which the variables are considered **Warm** or **Not very fast** is the degree to which the brake pressure is relaxed. Thus one fuzzy rule can replace many—often very many—conventional rules. And since fuzzy logic creates a control surface by combining rules and fuzzy sets, it allows designers to build controllers even when their understanding of the mathematical behavior of the system is incomplete.

> One fuzzy rule can replace many —often very many— conventional rules

So when is it appropriate to use fuzzy logic? When one or more of the control variables are continuous; when a mathematical model of the process does not exist, or exists but is too difficult to encode, or is too complex to be evaluated fast enough for real-time operation, or involves too much memory on the designated chip architecture; when high ambient noise levels must be dealt with or it is important to use inexpensive sensors and/or low-precision microcontrollers (since fuzzy logic's interpolation capabilities work well with 4- and 8-bit controllers); and perhaps above all, when an expert is available who can specify the rules underlying the system behavior and the fuzzy sets that represent the characteristics of each variable.

FUZZY MODEL. The components of conventional and fuzzy systems are quite alike, differing mainly in that fuzzy systems contain "fuzzifiers," which convert inputs into their fuzzy representations, and "defuzzifiers," which convert the output of the fuzzy process logic into "crisp" (numerically precise) solution variables [Fig. 1].

In a fuzzy system, the values of a fuzzified input execute all the rules in the knowledge repository that have the fuzzified input as part of their premise. This process generates a new fuzzy set representing each output or solution variable. Defuzzification creates a value for the output variable from that new fuzzy set.

For physical systems, the output value is often used to adjust the setting of an actuator that in turn adjusts the state of the physical system. The change is picked up by the sensors, and the entire process starts again.

In contrast, a PID controller is based on a rigorous mathematical model of some linear process [Fig. 1, bottom]. These models develop, by means of root locus or some other method, a set of equations that describe the stable equilibrium state of the control surface, with coefficients being assigned to the proportional, integral, and derivative aspects of the system. A PID controller reads a precise sensor value, applies the mathematical model, and produces a specific output from the mathematical algorithm.

While the PID model may seem the simpler and hence, the more economical representation, the contrary is more often true. Fuzzy controllers are in fact easier to prototype and implement, simpler to describe and verify, and can be maintained and extended with greater accuracy in less time. Moreover, because of their reliance on rules and knowledge, they give their environ-

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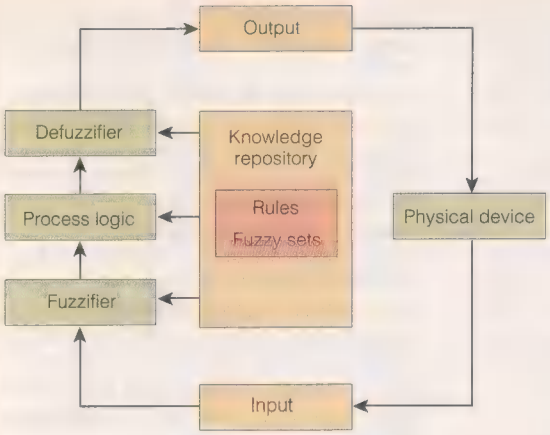
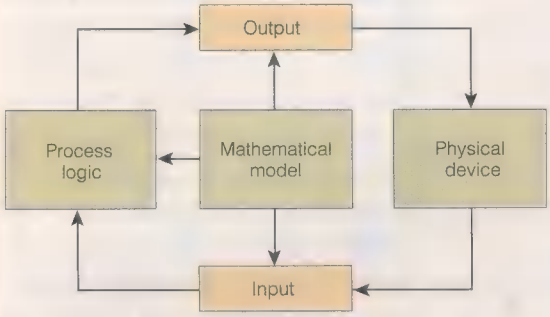
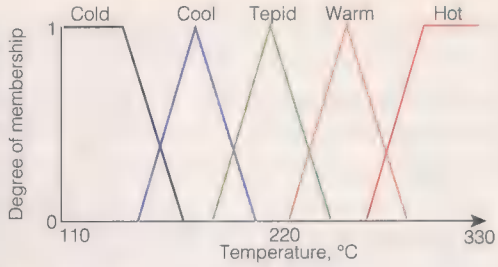
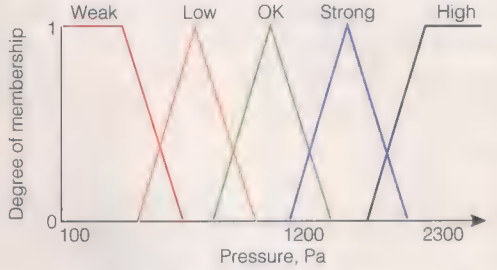


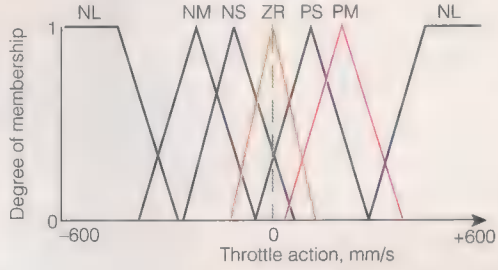


[1] In a typical fuzzy system [top left], the input is read from an external source and fuzzified before being processed by the fuzzy logic. The output of the process logic is defuzzified before being sent to the external physical system under control. A conventional control system [bottom left] has a very similar overall structure, but without the fuzzy elements.

*[2] Both the inputs (temperature and pressure) and the output (throttle action) are defined as fuzzy regions in a fuzzy logic system. For the throttle action variable, the regions are: negative large (**NL**), negative medium (**NM**), negative small (**NS**), zero (**ZR**), positive small (**PS**), positive medium (**PM**), and positive large (**PL**).*







ments what Lotfi Zadeh (the father of fuzzy logic) calls a higher "machine intelligence quotient."

STEAM TURBINE. The architecture of a simple fuzzy controller for a steam turbine shows how this process works. The design of the turbine's throttle action is based on two control variables: temperature and pressure. In order to build a controller that represents the relationship between the inputs and the output, each control variable must first be decomposed into a set of control regions [Fig. 2, top and middle] and the

Defining terms

Control variable: a variable that appears in the premise of a rule and therefore controls the state of the solution variable.

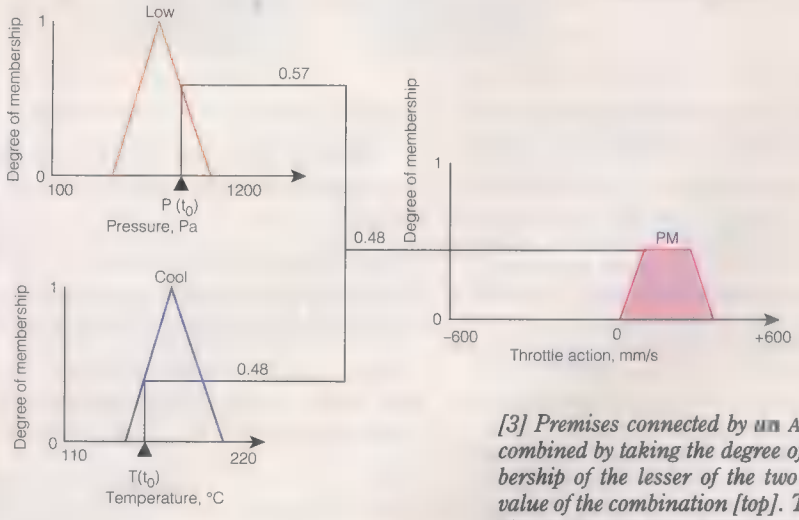
Defuzzification: the process of converting an output fuzzy set for a solution variable into a single value that can be used as an output.

Fuzzy set: a set that allows partial membership states. Ordinary, or crisp, sets have only two membership states: inclusion and exclusion; fuzzy states allow degrees of membership as well.

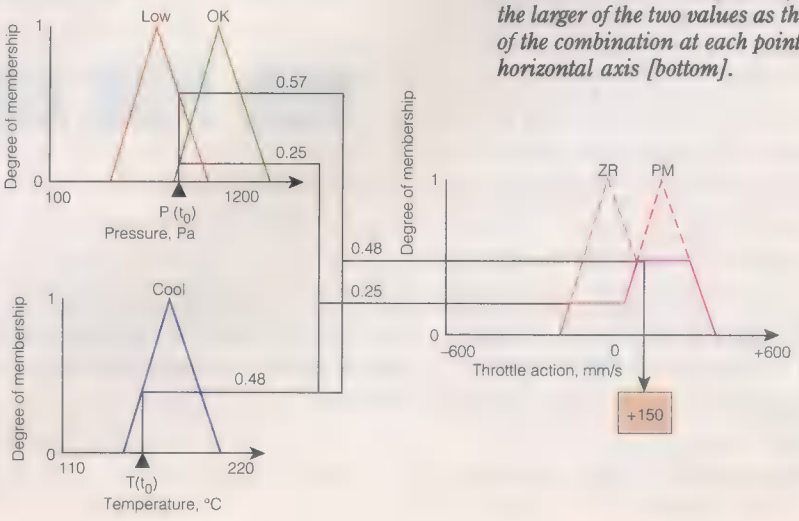
Overlap: the degree to which the domain of one fuzzy set overlaps with that of another. As an example, the right-hand edge of a Cool fuzzy set may overlap the left-hand edge of a fuzzy set called Warm, so that some temperatures belong in both sets.

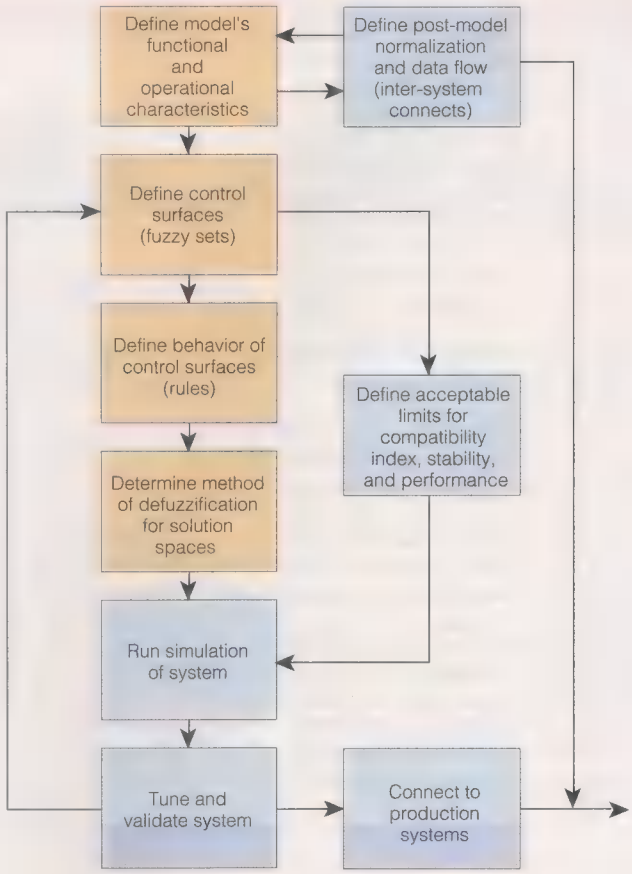
Solution fuzzy set: a temporary fuzzy set created by the fuzzy model to resolve the value of a corresponding solution variable. When all the rules have been fired, the solution fuzzy set is defuzzified into the actual solution variable.

Solution variable: the variable whose value the fuzzy logic system is meant to find.



[3] Premises connected by AND are combined by taking the degree of membership of the lesser of the two as the value of the combination [top]. To combine rules, OR them together by taking the larger of the two values as the value of the combination at each point on the horizontal axis [bottom].





[4] Most successful fuzzy logic development projects follow an iterative development cycle like this. The pink boxes represent the four central steps in the design process.

output or solution variable then redefined into a set of fuzzy regions [Fig. 2, bottom].

When the fuzzy sets have been defined, the conceptual model is completed by writing the rules that describe the action taken on each combination of control variables. Some of these rules might appear as:

1. *If temperature is* **Cool** *AND pressure is* **Weak**, *then throttle action is* **PL**.

2. *If temperate is* **Cool** *AND pressure is* **Low**, *then throttle action is* **PM**.

3. *If temperature is* **Cool** *AND pressure is* **OK**, *then throttle action is* **ZR**.

4. *If temperature is* **Cool** *AND pressure is* **Strong**, *then throttle action is* **NM**.

What is needed to complete this example is a means for converting these input fuzzy sets and rules into an output fuzzy set, and then into a crisp output for controlling the throttle. Note that a fuzzy model is, in a sense, a parallel processor. All the rules that have any truth in their premises will fire and contribute to the output fuzzy set—the one that will represent the throttle action control variable in the steam turbine example.

Suppose that at given time, t_o, the system sensors determine the turbine pressure to be $P(t_o)$ and the temperature to be $T(t_o)$ [Fig. 3]. As the figure shows, $T(t_o)$ falls into a single region of the T variable—namely **Cool**. But $P(t_o)$ has degrees of membership in two regions of its fuzzy set—**Low** and **OK**. This combination causes rules No. 2 and No. 3 to fire.

The two rules have somehow to be combined to form a single system output. The following three-step procedure shows how:

- For each premise expression connected by an AND, take the minimum of the truth of the expressions as the truth level of the premise.
- Truncate the output fuzzy set being built at the truth level of the premise.
- Copy the newly modified fuzzy set into the output variable's fuzzy set. If that region is not empty, combine it with the current contents by taking the maximum of the new fuzzy region and the currently existing fuzzy region at each point in the domain (along the horizontal axis.) In other words, if the region is not empty, then OR the outputs together.

Returning to the steam turbine example, vis-à-vis rule No.2 (*If temperature is* **Cool** *AND pressure is* **Low**, *then throttle action is* **PM**), it may be seen that T has a 0.48 degree of membership in **Cool** and P has a 0.57 degree of membership in **Low**. In accordance with the first step of the procedure, therefore, the lesser of the two figures—namely, 0.48—is taken as the truth level of the premise. Then, in accordance with the second step, the level of the output of rule No. 2—namely, **PM**—is truncated at that level, and copied to the output variable fuzzy set [Fig. 3, top].

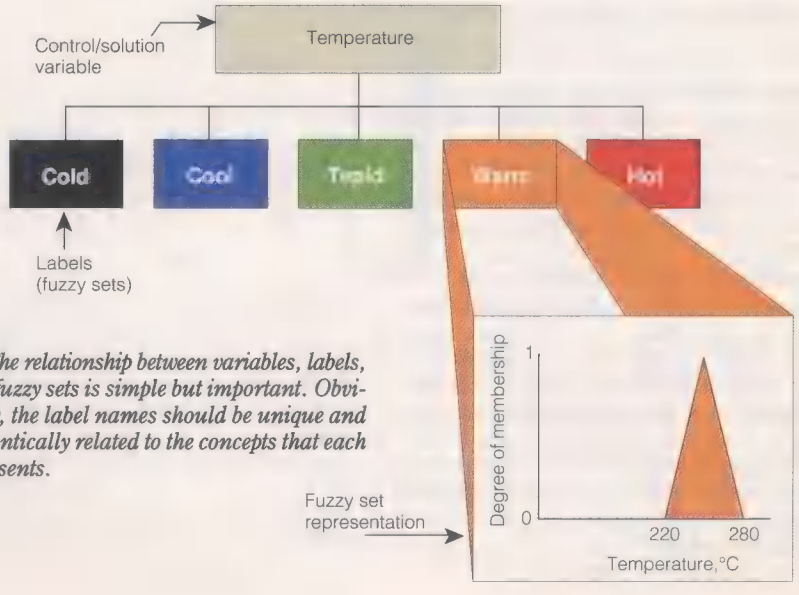
When rule No. 3 fires, the **ZR** fuzzy set is also truncated at the truth of its premise (the lesser of 0.25 and 0.48) and then copied into the output throttle action region. But since the region is not empty, this modified fuzzy set is combined with the **PM** fuzzy set by taking the maximum of their respective membership grades at each point along the horizontal axis [Fig. 3, bottom].

From this combined region, one of the several techniques of defuzzification is applied to produce an expected value for the throttle action. In this case, using the center of gravity, or centroid, of the combined region, a value of +150 mm/s is produced.

This value is used to adjust the throttle. After that, the pressure and temperature sensors will make new measurements, starting the cycle over again.

METHODOLOGIES. Although the previous example illustrated how fuzzy systems work, it gave few hints on how to specify, develop, and deliver one. Yet it is important to have a good design methodology for fuzzy systems if only because they are new to most designers, who therefore have no hoard of experience on which to rely for guidance.

Fuzzy models, be they employed in process control or information technology, tend to follow the same application development



[5] The relationship between variables, labels, and fuzzy sets is simple but important. Obviously, the label names should be unique and semantically related to the concepts that each represents.

cycle [Fig. 4]. The methodology attempts to formalize and structure a procedure in which the conceptual design is done on paper, and the later steps are an iterative cycle of modeling and simulation, carried out on a computer using fuzzy logic development tools, and continued until the model behaves as desired.

It cannot be overemphasized that the paper portion of the process is critical: understanding the mechanics behind a system's behavior, and identifying the system dynamics in terms of the conventional input-process-output model is an absolutely essential part of fuzzy system design.

FOUR STEPS. Four of the steps in the cycle illustrated in Fig. 4 are central to this process. In the first, "Define the model functional and operational characteristics," the goal is to establish the architectural characteristics of the system, and also to define the specific operating properties of the proposed fuzzy model. The system is always described in terms of an input-process-output model. The first step in designing a fuzzy system follows the analysis techniques used by commercial application systems analysts and intelligent-systems knowledge engineers.

The fuzzy system designer's task lies in defining what information (data points) flows into the system, what basic transformations are performed on the data, and what data elements are output from the system. Even if the designer lacks a mathematical model of the system process, it is essential that she have a deep understanding of these three phenomena. This step is also the time to define exactly where the fuzzy subsystem fits into the total system architecture, which provides a clear picture of how inputs and outputs flow to and from the subsystem.

Locating the fuzzy subsystem within the overall system helps the designer estimate the numbers and ranges of inputs and outputs that will be required. It also reinforces the input-process-output design step. And it is usually best done before tackling the details of input and output since the latter may well be affected by the localization.

In the second step, "define the control surfaces," each control and solution variable in the fuzzy model is decomposed into a set of fuzzy regions. These regions are given unique names, called labels, within the domain of the variable. Finally, a fuzzy set that semantically represents the concept associated with the label is created [Fig. 5].

Some rules of thumb help in defining fuzzy sets. First, the number of labels associated with a variable should generally be an odd number between five and nine. Second, each label should overlap somewhat with its neighbors. This overlap, in fact, is what gives a fuzzy controller its smooth, stable surface. The overlap should be between 10 and 50 percent of the neighboring space, and the sum of the vertical points of the overlap should always be less than one.

Finally, the density of the fuzzy sets should be highest around the optimal control point of the system and should thin out as the distance from that point increases. This rule was clearly applied in the throttle action variable of the steam turbine example, where the labels are bunched together in the middle of the domain but are more widely spaced toward the edges.

The third step, "define the behavior of the control surfaces," involves writing the rules that tie the input values to the output model properties. These rules are expressed in an English-like language with a syntax like:

> Fuzzy logic fits best when variables are continuous and/or mathematical models do not exist

►*If* <*fuzzy proposition*>, *then* <*fuzzy proposition*>,

where the fuzzy propositions are of the form, "*x* is **Y**" or "*x* is not **Y**," *x* being a scalar variable and **Y** being a fuzzy set associated with that variable.

Such a group of rules forms a fuzzy associative memory. When a set of input values are read, each of the rules that has any truth in its premise will be executed. Since these rules are declarative rather than procedural, their order in the knowledge repository is unimportant. Nevertheless, in the interests of maintainability, it is recommended that the rules be grouped by their premise control variables.

Generally, the number of rules a system requires is simply related to the number of control variables. The steam turbine system, for example, has two control variables, temperature and pressure, each of which is divided into five fuzzy regions. Since there are a total of 25 possible input combinations, the system requires 25 rules.

In some cases, it is possible to use fewer rules, but there are dangers in so doing. The rules represent knowledge, so if any are deleted, knowledge is removed from the system—knowledge that may become important if the system is later modified.

The fourth of the central steps, "select a method of defuzzification," is the final part of creating the basic fuzzy model. There are several ways to convert an output fuzzy set into a crisp solution variable, but the two most common are the composite maximum and the composite moment, or centroid.

The centroid method takes the center of gravity of the final fuzzy space and produces a result that is sensitive to all the rules—in particular, the results tend to move smoothly across the control surface. The composite maximum, on the other hand, produces a result that is sensitive to the truth produced by the single rule that has the highest predicate truth. By and large, process control applications use centroid, while information-based applications like risk evaluation and terrain analysis use the composite maximum.

Once the fuzzy model has been constructed, the process of simulation and protocycling begins. In this adjunct to the methodology, the model is compared against known test cases to validate its results. When the results are not as desired, changes are made either to the fuzzy set descriptions or to the mappings encoded in the rules.

Tools are available to help project managers and system designers evaluate fuzzy models and isolate problems at the fuzzy set or rule level. These tools measure such factors as the statistical compatibility between the model and test-bed data, and the stability of the model based on a loss of information. In general, though, a methodology will only be as good as the designer's understanding of the problem.

TO PROBE FURTHER. For an excellent introduction to fuzzy logic, readers may want to consider a US $195 education kit from Motorola Inc., which contains a PC-based introductory course (on both 5.25- and 3.5-inch disks), a demonstration version of Aptronix Inc.'s fuzzy inference development environment (FIDE, pronounced feeday), and a collection of fuzzy logic freeware with documentation. Further information on the kit may be obtained by writing Fuzzy logic, Box 600, Mail Drop F30, Austin, Texas 78762, or calling Norma Williams at 512-505-8101.

Fuzzy Sets, Uncertainty, and Information by George J. Klir and Tina A. Folger (Prentice Hall, Englewood Cliffs, N.J., 1988) is an especially readable and well thought-out presentation of fuzzy logic as it relates to information modeling. Unlike the majority of recent books on the subject, it does not delve deeply into complex mathematics (although it certainly covers the mathematics of fuzzy logic) and it is not concerned exclusively with process control.

Another excellent text is *Neural Networks and Fuzzy Systems—A Dynamical Systems Approach to Machine Intelligence* by B. Kosko (Prentice Hall, Englewood Cliffs, N.J., 1992), which is especially good on the overlapping of the labels of a variable. Kosko shows that Aristotelian and Boolean logic are special cases of fuzzy logic. He also does a good job of presenting the differences between probability and possibility theory.

ABOUT THE AUTHOR. Earl Cox is the founder and chief executive officer of the Metus Systems Group, an advanced systems science consulting and software services organization in Chappaqua, N.Y. Prior to that, he founded Knowledge Based Technologies, where he developed Telus, a mainframe-based fuzzy logic expert system.

Consolidating European power

Synchronous coupling of the power grids on either side of the former iron curtain makes economic sense

More than any other consumer good or service, electric energy flowing through a large interconnected multinational system makes for solidarity among the countries that use it. In Europe, this solidarity will develop and broaden in scope the next few years, as the plans to increase the electric energy exchange between its eastern and western halves go into effect. The reciprocal solidarity ranges from the very long term to a few seconds—from the design of the architecture of the system to the prevention of serious incidents that could have repercussions throughout the continent. The potential benefit from such an exchange, if done economically, is substantial—all the participating countries together could save up to a total of a few hundred million European Currency Units every year. (There is about 0.7 ECU to the 1992 U.S. dollar.)

ELECTRIC CURTAIN. After World War II, the iron curtain went up, dividing Europe into two blocs. The Cold War mentality affected the electric systems in Europe, and energy exchanges between the blocs fell to practically nil. The political iron curtain became also an electric curtain.

However, the allure of safer and cheaper energy from electric interconnection was strong. In the east as in the west, national grids were beginning to operate in parallel with their neighbors.

On the western side, the German, Swiss, and French networks began operating in parallel in 1957, others joined later, and today, members of the Union for the Coordination of Production and Transmission of Electricity (UCPTE) are operating synchronized systems—working at the same frequency. The union, now based in Arnhem, the Netherlands, has 12 members: Portugal, Spain, and France, with Belgium, the Netherlands, and Luxembourg, plus West Germany, Switzerland, Austria, Italy, Yugoslavia, and Greece. Albania and the continental part of Denmark (Jutland) have joined the synchronized system, but not the UCPTE. The whole list represents a peak demand of 220 000 MW.

Meanwhile, in eastern Europe, Hungary was connected to Czechoslovakia in 1953, and in 1962 East Germany, Hungary, Czechoslovakia, Poland, and the western part of Ukraine were synchronized. Romania joined them a year later, followed by Bulgaria in 1967. And in 1988, the Soviet system linked up with the Ukrainian system; the result resembles the UCPTE in power level but not in geographical coverage—it spans over 7000 km to Lake Baikal.

As for northern Europe, Finland, Sweden, Norway, and Seeland, an island part of Denmark, are interconnected today. But the sea blocks any thought of synchronous interconnection with the rest of the continent. Several high-voltage dc (HVDC) links join Norway and Sweden to the UCPTE system.

Because of the political barrier between Eastern and Western Europe, which lasted for nearly half a century, exchanges between them even in terms of electric energy were discouraged. Consequently, the two blocs developed separately at the same rated frequency of 50 Hz, but not in synchronism, that is, with no power lines linking the two systems directly.

> With a mere trickle of energy flowing through it, the old iron curtain was, in effect, an excellent insulator

Synchronized operation means that all generators producing the same frequency operate at exactly the same speed (rotation speed determines frequency) and that the angular positions of the rotors are linked by a synchronizing electric torque. Control of the speed of all generators must be well coordinated. It must also be consistent with the way in which each country undertakes its fair share of the tight maintenance of frequency, that is, in the construction of a balance between total demand and supply. Frequency remains at 50 Hz only if supply equals demand. If, for instance, the instantaneous consumption goes up, the missing energy is taken from the rotating machines—turbines and the generators—and the machines slow down, causing a drop in frequency until additional power is supplied to the turbines.

As the years went by, the two systems became more at odds technologically, a state of affairs reflected in sizeable differences in operating standards. Frequency control, in particular, which realizes a permanent matching of supply and demand, conformed to a much higher standard on one side than the other. These differences prevented the systems' parallel operation.

Around 1975, many discussions took place in Geneva, Switzerland, as part of the United Nations' Economic Commission for Europe, to advance the synchronization of both parts of Europe, but to no avail. In fact, though, since experts on either side of a border always find great technical and economic interest in trading electric energy, two types of barter developed along the iron curtain: exchanges in pockets and by ac/dc converter stations.

EXCHANGES IN POCKETS. A pocket is an enclave in a system belonging territorially to synchronized system A but connected electrically with another synchronized system B. Part of the production or consumption of system A is therefore synchronized with system B [Fig. 1]. Naturally, this enclave is not electrically connected to the remainder of A. Pockets of production or consumption or a mixture of both can be imagined. This problem of pockets explains why a fair number of electric lines cross the old iron curtain today. However, the effective power transmitted is nowhere near line capacity, because the pockets are quite difficult to manage electrically.

AC/DC EXCHANGES. When ac at 50 Hz is converted to dc and back again at the same frequency, the link formed is asynchronous, in that the two electric systems thus joined are not synchronized. This technique is used for some energy exchanges between, on the one hand, Czechoslovakia and Austria (550 MW) and on the other, Russia and Finland (1000 MW). Other converter station projects are presently under way, between Austria and Hungary and between Germany and Czechoslovakia. Unfortunately, the high cost of these stations inhibits the natural desire

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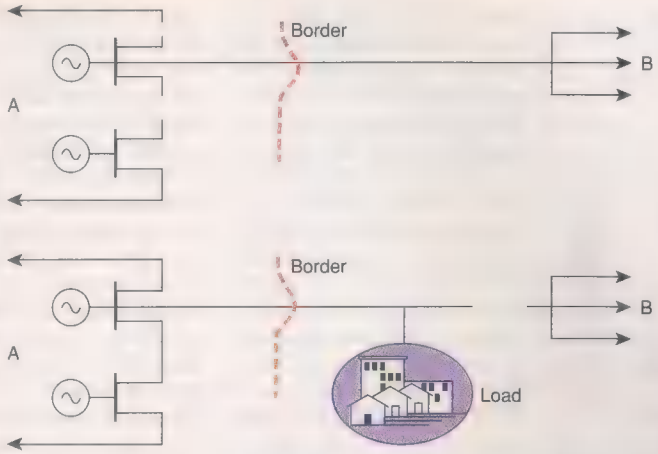


[1] Part of power system A to the left of the border between two countries forms a pocket that is synchronized with system B to the right [top]. Alternatively, the residential load to the right of the border may form a pocket synchronized with system A.

to exchange electric energy over borders. In contrast, the pocket is cost free (except the ac lines), but allows exchanges only on a limited scale and over short distances.

PRESENT PROBLEM. The Cold War is at last over, and Europeans to the west and east are envisioning new relationships. One upshot should be a surge in the flow of electric energy between both parties. The problem is whether to continue these exchanges over dc converter stations or whether it is possible and desirable to synchronize the systems to ensure least-cost energy exchanges and greater political and economic solidarity between the nations involved.

Today, the topology of the flows of electric energy (ac and dc) indicates four typical groups of national borders of particular interest: to the east, the border between the former Soviet Union (most of which is now the Commonwealth of Independent States) and Central European countries; next, the old iron curtain; then, a border running through roughly the middle of Western Europe; and finally, the border between the France-Spain-Portugal block and the remainder of Europe [Fig. 2]. The figure prompts several observations. First, the influence of large exporters of energy such as France or the former Soviet Union is obvious. Curiously enough, both countries export similar quantities, although for radically different reasons: commercial in the West, mutual economic cooperation in the East.

The mid-West-European border is a normal one between countries that have signed no large import or export contracts, but conduct classical emergency exchanges (in the event of temporary shortages) or economic exchanges (to reduce the overall cost of the energy produced by drawing on another's production facilities or demand curves). This border therefore gives an idea of the flow of exchanges that the countries are naturally inclined to foster, to benefit from the compensation phenomena possible through interconnection. It is not chance that exchanges are nearly balanced on both sides.

Because the four types of frontiers have different lengths, it makes good electrical sense to illustrate the density of exchanges in terms of megawatthours per kilometer of border [Fig. 3]. Compensation phenomena tend to link exchange densities to production and consumption densities. (The higher of the two flows is taken each time because it represents the exchange capacity between systems.)

As East European economies and industries rise to about the same level as in Western Europe, they will need to exchange ever higher power densities with the western countries, until these exchanges have reached a level at least 10 times that of today. This level simply reflects the quest for the benefit provided by the classical phenomenon of the interconnection of systems. Additional exchanges could arise from time differences between countries. And if these countries become large exporters to or importers from the West, the volume of exchanges could be markedly higher.

EAST-WEST CONTRACTS LIKELY? The key question is whether it is likely that large trade contracts will in the future be signed throughout Europe, especially across the old iron curtain. It is well known that it costs more to transmit electric energy than to transport primary fuel, and it is also sometimes more difficult to transmit electric energy because few people enjoy the eyesore of extrahigh-voltage (EHV) lines.

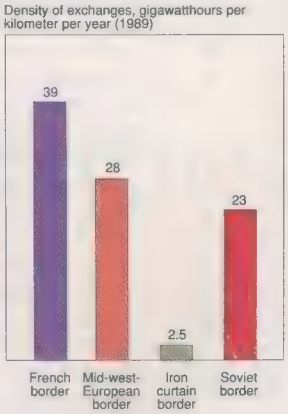
Nevertheless, popular opposition makes it difficult to build generating plants, whether nuclear, thermal or hydroelectric, in some countries, notably Italy and Switzerland. These nations are therefore forced to buy electric energy, in far from negligible quantities, from other countries and are presently hoping to turn to central or east European countries for their supplies.

As things stand, the last countries lack adequate installed capacity because many power plants there are obsolete. Nor are they organized, either financially or industrially, to build the missing generating facilities rapidly. They are envisioning collaboration with West European utilities, which would provide capital and know-how in return for sending part of the new generated power to Western Europe.

Although not a certainty today, it can be predicted that long-term electric energy exchange contracts will be signed between Eastern and Western Europe, increasing the need for exchanges between these two regions. Some specific projects—for example, between Russia and Germany—are under study.

However, these projects are somewhat

[2] The former Soviet Union as well as France exported 34 terawatthours apiece in 1989. The former Eastern Bloc had a surplus export of 34 TWh in 1989. The border running through the middle of western Europe represents mostly emerging exchanges, rather than major power export contracts. (Source: 1989 UCPTE.)



[3] The border between Eastern and Western Europe has the lowest annual electrical energy exchange density—only 2.5 gigawatthours per kilometer each year, as compared to 39 GWh/(kmxyear) along the borders between Spain, France, and the United Kingdom to the west and Italy, Switzerland, Germany, Luxemburg and Belgium to the east.

contrived in that transmitting electricity over long distances is expensive and difficult, and the importing country must worry about the safety of the energy supply. In addition, it poses general security problems for European countries at large: the sudden outage of an important transmission line in Europe would subject more than one country to instantaneous repercussions, events that utilities are unsure they can fully master. In the long term, the most likely thing is that collective wisdom should prevail, with each country resuming a policy of self-sufficiency, and with national electric output roughly meeting national demand.

Despite the above, the East-West electric energy flows are bound to increase in the future by at least a factor of 10. If so, planners will have to determine whether this increase will have to be carried by costly ac/dc converter stations or whether the synchronization of both systems would obviate the need for them.

AC AND DC INTERCONNECTION. Schematically, the dc technique can be used in two ways: without or with dc lines. The first is the way it is done today, using back-to-back stations along the old border between Eastern and Western Europe, with one and the same building housing both ac/dc and dc/ac conversion stations, so that no dc line is needed. These stations would be strung along the border between the synchronized systems. The other approach is to build one or several dc lines, penetrating some distance into both synchronized systems to form so-called "staples." The conversion stations are then at either end of the line and also, if necessary, at intermediate points, forming a multiterminal configuration.

One advantage of back-to-back converter stations is their total control over electric power flowing through the two electric systems they join, while in the event of a serious incident, they provide an additional degree of freedom in preventing cascading collapses. Each of the systems connected by back-to-back converter stations must be responsible for its own frequency control.

To some extent, these converter stations, insofar as they are not too numerous, uncouple the problems and simplify the necessary real-time coordination of system management. Their main drawback is their cost. For example, the energy cost penalty due to the use of these stations is approximately 0.5 percent of an ECU per kilowatthour. Consequently, only a few countries can afford them. East-West transfers would then flow through rather few points—an undesirable situation for both technical and political reasons. Free trade in electricity would be markedly reduced and European solidarity would suffer.

STAPLED SYSTEMS. Like the back-to-back configuration, the stapling together of two systems by dc lines gives good control of power flow between the systems. Also, dc lines themselves are cheaper than ac lines because the insulation voltage for the dc lines is lower by a factor of the square root of 2—the ratio of maximum (peak) to effective voltage. And when dc lines are at least 700 km long, the expense associated with the converter stations can be justified. Another advantage is the option of laying relatively short dc transmission cables underground in those areas where the topography is extremely unsuited to overhead lines. Because of the high cost involved, however, this option should be limited to only a few locations. All of the above make stapled systems adequate for long-distance power exchanges.

The construction of long high-power lines, however, hinges on accurate knowledge of the trend of electric energy flows in Europe over the next 20 years. Such a forecast is not readily available. Nor are long high-power dc lines very suitable for natural compensation flows of the kind mentioned earlier, since these flows vary over time in both magnitude and direction. The meshed system, comprising many interlinked meshes, is far better adapted to these flows.

Stapled systems also are expensive, and difficult technical problems are encountered in building intermediate conversion stations along the dc transmission lines, wherever power exchanges are needed. Without these intermediate stations, the risk is that electric energy will be transmitted unnecessarily from one end of the line to the other and some or all of it will have to be sent part of the way back over the underlying network.

Then there is the security of the general system. When the sudden outage of a trans-european transmission line causes disruptions, it must be possible to control it fully.

Finally, the high level of power concentration required for the economic viability of the project—typically at least 3000 MW—is even more obvious than in the case of back-to-back stations. This concentration is not helpful either to general security or to the organization of energy flows from any point in Europe to another.

EXISTING AC LINES. Most of the ac transmission lines that would be used in East-West power exchanges are in place. It will be possible, at reasonable cost, to organize elec-

[4] Numerous ac transmission lines from 110 to 380 kV already exist along the border line between Eastern and Western Europe, including the former border between East and West Germany (not shown). These, along with two back-to-back converter stations now under construction—between Czechoslovakia and Germany and between Hungary and Austria—are likely to increase power exchange along the border.

tricity exchanges between all regions on either side of the former East-West border. In general, the existing ac transmission lines allow a better coordination between systems on both sides of the border, at optimized cost, and in a far more flexible manner than the dc systems would allow.

Ac connection would conduce to the creation of a very large synchronous system. As a result, utilities on both sides of the border would have to overcome the increased complexity of the organizations of the different utilities.

COLLABORATION. International collaboration on this important technical issue is essential. Within an interconnected electric system, a stable frequency is a common resource that must be managed collectively. Patient, joint development of general guidelines is a must.

Once general guidelines have been set, the modalities of implementation of East-West power exchanges are subject to bilateral negotiations between countries with common frontiers. The Paris-based International Union of Producers and Distributors of Electrical Energy (Unipede), speaking through its Large Systems and International Interconnections Study Committee, in March 1990 agreed with UCPTE to create an *ad hoc* working group, common to both organizations. This group is responsible for examining the whole issue, and more particularly, for indicating whether ac connection is technically possible, and if so, when and under what conditions.

This group was the first extraordinary exchange forum for experts from both sides of the former iron curtain. They were unaccustomed to speaking to each other, let alone to exchanging technical views on how their systems operate. In addition to Western and Northern European representatives, this group comprises representatives from Czechoslovakia, Hungary, Poland, the Commonwealth of Independent States (the former Soviet Union), Bulgaria, Romania, Yugoslavia, and Turkey.

From the many discussions that took place, it became clear that synchronous interconnection of Europe as a whole is desirable after the following points have been solved:

- The Commonwealth of Independent States (CIS) is at present handling frequency control for the whole East European system. The interconnection of UCPTE and East European countries, unaided by CIS, would therefore require the Easterners to implement a frequency control as efficient as that of the UCPTE. Doing this could involve the construction of additional generating sets. More generally, countries that are candidates for entry into the synchronized system should offer the same reliability and same standard of service as those of Western countries.
- Given the magnitude of the new Commonwealth's electric system (the power level of its grid is equivalent to that of all UCPTE countries put together), the system forms a special case that needs to be examined separately. This study has not yet been finished by the group. Because the extension to the synchronous system will have to be organized progressively, initial couplings are unlikely to include the Commonwealth.
- That situation underscores the problem of such countries as Hungary and Bulgaria. As part of old contracts, they continuously receive a share of their electric energy from the CIS. They cannot be synchronized with both the UCPTE and the Commonwealth. The problem of imports from the Commonwealth is therefore a little annoying. It could be solved by preserving the pockets in countries such as Hungary, Bulgaria, and to a far lesser extent, Czechoslovakia, letting them remain synchronized with the Commonwealth grid; then the rest of the country could be synchronized with the UCPTE, by installing back-to-back dc stations at the end of the lines coming from the Commonwealth. The ideal situation would of course be to dismantle the stations located near the present UCPTE border and to re-assemble them closer to the old USSR border line, an act that may save approximately 50 percent of the cost. However, this problem is temporarily less acute, due to the decline in consumption in Hungary and Bulgaria.
- Although there are numerous transmission lines that connect Eastern and Western Europe [Fig. 4], the eastern and western systems have each been structured to meet the exchanges specific to them. The interconnection of the two grids could cause undesirable loop transfers (transfers due to the Kirchoff law rather than the will of the dispatcher) and necessitate a change in the internal structure of these systems. This possibility is presently under study. Austria has already undertaken initial calculations that show how a power flow through Europe is distributed amongst countries.
- The general security of the interconnected system should be examined and adequate protection installed to prevent a major incident from sweeping Europe from end to end.

The working group made its initial report to the Unipede Copenhagen Congress in June 1991. It concluded that synchronous coupling between the Eastern and Western Europe is possible provided that the technical problems mentioned earlier be solved beforehand. The group estimated the time needed to find solutions at 5–10 years.

THREE STAGES. A progressive approach is essential in this field, so that synchronization may have to follow three stages. First would come Czechoslovakia, Poland, and Hungary. Next would come countries like Bulgaria, Rumania, and Turkey. Finally, extensions would be possible into yet other countries.

The working group is continuing its studies and refining its analyses. It will be presenting its final conclusions within the next few months, because Europe is making history very quickly today, and those involved in electric power cannot afford to be left behind.

> Within an interconnected electric system, frequency must be democratically managed and collectively stabilized

The question of the long-term future of the European electric system is also posed in parallel to the problem of East-West interconnection. Will there really be large transfers of energy across Europe? How far can the synchronous system go? For example, the present intention is to extend it into North Africa. Is it now time to examine the usefulness of a higher voltage level? Should dc play a new role? Or will the 400-kV meshed system remain for now the basis of the European system? Another Unipede-UCPTE group is proposing to examine these issues, taking over from the initial group, but from the long-term point of view.

In conclusion, no one should underestimate the difficulties caused by the technical and cultural gap between the two parts of Europe or the self-interest with which each country views the problems. Much work has already been done, but the hardest part lies ahead. However, the interest of electric interconnections and the solidarity it represents is too great for experts in electricity not to achieve their goal, despite the upheavals yet to be expected from history.

TO PROBE FURTHER. The source paper for this article, "Cooperation in the field of electric systems and between Eastern and Western Europe," will appear in the multi-volume proceedings of the 15th World Energy Council (WEC) Congress. WEC scheduled this congress for Madrid, Sept. 20–25, 1992, on the theme of energy and life. For more information on the copyrighted article, contact WEC at 34 St. James's St., London SW1A 1HD, United Kingdom; (44+71) 930 3900; fax, (44+71) 925 0452.

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The art of systems architecting

The design of complex systems must blend the art of architecture with the science of engineering

Few engineers would be surprised, today, to see the word "architecture" in their professional journals; nor would they have to think twice about its meaning. Architecture is understood to be the underlying structure of things—whether of buildings, communication networks, neural networks, spacecraft, computers, software or organization charts—systems all.

Less recognized, perhaps, is that where there are architectures, there must be architects. Moreover, there must be a process, "architecting," by which the architectures are created, designed, and built.

Architecting, itself, has ancient roots. It first appeared in Egyptian writings some 4000 years ago. Many of its basic principles were codified by the Roman, Vitruvius, in the 1st century B.C. But only in the last 50 years or so has the concept of "systems" been comparably formalized.

The merging of architecting and systems into systems architecting is still more recent. That process is accelerating, driven by three factors: the increasing architectural complexity and scope of global-sized projects and markets, the ubiquity of computers in virtually all modern systems, and the power of computer aids to system design.

Retrospectively, it is apparent that the success or failure of many defense, space, and civil systems of the last half century has depended in large part on how they were structured. The most successful ones were conceived, built, tested, certified, and operated in a way that ensured their integrity and performance. They were based on a consistent set of principles and techniques that were maintained throughout all phases of the project. And their designs were resilient enough to bend to the inevitable changes brought about by time and circumstance.

As civil architects would say, they had good bones. They also had fine architects who supervised their programs from beginning to end. The systems that have failed—whether technologically, politically, or economically—lacked these essentials.

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Such conclusions are not new. Similar ones have been drawn over the centuries about pyramids, cathedrals, cities, ships, and fortifications. What is new is that those conclusions are now being seen as relevant to the engineering of electrotechnical systems.

Systems engineering and architecting are brought together by certain common principles. Each is concerned with complexity and reliability—systems engineering because of its nature and architecting because of its scope. The form of a system is strongly driven by the functions it is called upon to perform. Architecting defines that form by matching, fitting, balancing, and compromising proposed functions and forms until a practical result can be achieved.

SYSTEMS PRINCIPLES. Our first focus is on the principles of systems—an area more familiar to most engineers. Different people can mean different things by the word "system." For the purposes of architecting, a useful and sufficiently precise definition of a system is: "A collection of different things so related as to produce a result greater than what its parts, separately, could produce." Indeed, the purpose of building a system is to achieve that greater result.

Example: The system function of an assembled automobile is transportation, unavailable from the parts separately.

This definition of system has at least two important consequences. *First, all systems have subsystems and all systems are parts of larger systems.* Hence the systems world is inherently unbounded: no matter where a boundary might be drawn, things important to the system will exist outside it.

The same situation occurs in classical architecture.

Example: Designing a water faucet (a very small system, but a system nonetheless) means considering not only its own function, but also the demands of the systems within which it operates, such as the inclusion of urban water-usage restrictors to minimize the effects of drought on scenic lakes several hundred kilometers away.

Thus, complex systems cannot be architected, built, or operated in isolation. Their "outer" and "inner" worlds will always intrude. The best that can be done is to draw boundaries so that intrusions, when they occur, are secondary and not primary—that is, that they can be accommodated without breaking the system.

Example: The design of a manned spaceflight program, a strategic defense system, a national wideband communication network, an airline, or a light rail system is strongly influenced by extra-technical imperatives—economic, human, social, political, and international. These imperatives must be included in the design or the system will fail or abort, quite possibly well before completion. Placing them "outside" the system for design purposes could destroy any chance of success.

The architect's task is made particularly difficult by the fact that rarely, if ever, is there a single optimal solution for all parties and all circumstances. The objective, instead, is a kind of general satisfaction based on practicality, fit, balance, and compromise. As experienced architects will affirm, that takes both science and art.

The second architecturally relevant consequence of our definition of system is *the value added by a system must come from the relationships between the parts, not from the parts per se.* Each part already contributes its own inherent value to the system. But it is the total of all the parts working together that yields the whole system—a phenomenon sometimes known as synergism.

Example: The Douglas Aircraft DC-3, the first commercial airliner to make a profit for its owners, consisted of airfoils from the National Advisory Committee on Aeronautics (the predecessor to the U.S. National Aeronautics and Space Administration), monocoque designs already tried by the Boeing Aircraft Co., engines on the shelf, and control systems then in development. But, with modified elements in novel combination, the DC-3 made air travel efficient, reliable, and pleasurable.

It follows that *systems architects who work with systems must be specialists in relationships—not generalists who know a little bit about all the parts.* Their specialty is

Defining terms

Architecting: the process by which a system is created, designed, and built.

Heuristics: empirical rules of thumb derived from experience and judgment, useful for attacking problems too complex to be solved by analytical techniques alone.

System: a collection of different things related in such a way as to produce a result greater than what its parts, separately, could produce.

Systems architecture: the underlying structure of a system, such as a communication network, a neural network, a spacecraft, a computer, major software, or an organization.

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concentration on the system as a whole: that is, on those elements, interfaces, and factors that have the most effect on overall system performance, cost, and schedule. Systems architects must necessarily know, or learn, a great deal about some details—those that impinge on the overall system—but need not, and probably should not, pay much attention to the rest, which are best handled by the subsystem experts with whom the systems specialists work.

Example: A launch vehicle systems engineer need not know the detailed design of a solid rocket motor. But that systems engineer would be expected to understand in some detail how the rocket's segments were connected, how each rocket was attached to others and to the payload, what its performance tolerances must be compared to other rockets on the same vehicle, what control authority is provided by its thrust control mechanisms, and so forth.

Without question, it requires expertise to know which details, interfaces, tradeoffs, and compromises count the most and which, the least. Poor choices can be disastrous; too many choices can be overwhelming.

ART AND SCIENCE. Much more so than engineering, architecting is an art as well as a science. There is an art to creating any structure, whether a building, a ship, a spacecraft, a network, or any other system. It is not just a figure of speech to praise a system as elegant or as having style.

The artistic element of architecting is most apparent when architects are asked how they create what they do, how they come up with alternatives out of the blue that withstand the scrutiny of analyses, and how they know that when all the parts come together, a system never built before will work to a client's satisfaction.

The usual, and not very helpful, answer is, "I just use common sense." Further inquiry leads to the discovery that what is really meant is contextual sense: doing what is sensible in the context of the problem. Commercial aircraft architects do it in creating a safe and profitable aircraft, spacecraft architects in producing a reliable and efficient spacecraft, and software architects in developing powerful and user-friendly software. And that means the use of empirical insights, tricks of the trade, and lessons learned from past successes and failures—that is, heuristics.

The art in architecting is a special process, essential in treating situations too complex for analysis. It evolved centuries ago as a way to handle ill-structured problems with all their uncertainties, unknowns, conflicting requirements, and sociopolitical imperatives—problems typical of complex systems.

At the risk of oversimplification, discipline-oriented engineering is deductive, analytical, and rational, while systems-oriented architecting is inductive, intuitive, synthetical, and pragmatic. At one extreme are the powerful applied science tools of engineering; at the other are the often personal arts of architecting. Straddling both is the practice of systems engineering.

Architects of buildings who have studied the process of architecting—how architects work—have identified four methods in common use that depend on the nature and phase of the project, the particular problem to be solved, and the style of the architect:

Normative methodology relies on standard, quantitative solutions based on subjective value judgments ("good" vs. "bad" practice). Building codes, communication protocols, and design handbooks are examples.

Rational methodology is based on quantitative analysis and algorithms that tell how to find a solution, but not what it is. The scientific method of data gathering, hypothesis, and test is an example. Calculus is another. Rational methodology—the mainstay of systems engineering—is intended to be as objective as possible. Optimization is one of its goals.

Argumentative methodology is based on broad participation of interested parties. Brainstorming is one of its techniques; quality circles is another. This methodology aims for imaginative consensus. Its strength is group commitment to a common goal.

Heuristic methodology is based on common sense or rules of thumb derived from experience and judgment. The law of supply and demand is an example from economics. Murphy's Law is an example from system design. The aim here is reasonable, satisfactory solutions and an avoidance of system-level disasters. More than the other three methodologies, the heuristic methodology is an art.

The normative and rational methodologies are widely taught in engineering schools and used extensively in practice. These methods have powerful tools available—statistics, probability theory, modeling, optimization, tradeoff charts, simulation, statistics, operations research, and performance analysis. They help break down problems into solvable subproblems whose solutions are then integrated into the whole. System certification is quantitative and not easily disputed. These two methodologies comprise the "science" part of architecting and the technical foundation of systems engineering, detailed design, and integration.

In argumentative methodology, free-ranging discussion reigns. Its weakness is design by committee. On the surface, it seems to contradict a widely held view that the best architectures are the product of a single mind or small team. Success, therefore, requires good team dynamics—a well-designed human system guided by the empirical knowledge of human behavior. In this respect, the argumentative methodology might be considered a managerial variation of the more general heuristic method.

HEURISTICS UNBOUND. The heuristic methodology is particularly characteristic of architecting. In contrast with the other methodologies, it is synthetical, inductive, and experiential. Its tools are heuristics—rules of thumb for discarding out of hand unreasonable options, for maintaining the integrity of system goals, for taking precautions against pitfalls ahead, and for recalling lessons learned.

But most important, heuristics is the only methodology that

Some heuristics for building a system

The conceptual phase:

- The choice between architectures may well depend upon which set of drawbacks the client can handle best.
- Extreme requirements should remain under challenge throughout system design, implementation, and operation.
- Don't assume that the original statement of the problem is necessarily the best or even the right one.
- No complex system can be optimum to all parties concerned, nor all functions optimized.
- A model is not reality.
- Complex systems will develop and evolve within an overall architecture much more rapidly if there are stable intermediate forms than if there are not.
- Build in and maintain options as long as possible.
- Don't make an architecture too smart for its own good.

The build and test phases:

- The product and process must match.
- An element good enough in a small system is unlikely to be good enough in a more complex one.
- Within the same class of products and processes, the failure rate of a product is linearly proportional to its cost.
- High-quality, reliable systems are produced by high-quality architecting, engineering, design, and manufacture, not by inspection, test, and rework.
- Regardless of what has gone before, the acceptance criteria determine what is actually built.
- To be tested, a system must be designed to be tested.
- Qualification and acceptance tests must be both definitive and passable.
- The cost to find and fix a failed part (or software bug) increases by an order of magnitude as that part is successively incorporated into higher levels in the system.

The operations phase:

- Before the flight, it's opinion. After the flight, it's obvious.
- The first quick-look failure analyses are often wrong.
- For every competitive system, there is a countersystem.
- Success is defined by the beholder, not the architect.
- There's nothing like being the first success.

Systems Architecting: Creating and Building Complex Systems, by Eberhardt Rechtin, published by Prentice Hall, Englewood Cliffs, N.J., 1991.

directly attacks problems too complex to be solved by analytical techniques alone; that is, those characteristic of unbounded systems.

A good example of a descriptive heuristic, mentioned earlier, is Murphy's Law: "If something can go wrong, it will." An associated prescriptive heuristic, an antidote to Murphy's Law, is: "Simplify, simplify, simplify." Neither of these mentions statistics or statistical quality control. Instead, they suggest a strategy: if a system is built in such a way that something could possibly go wrong, no matter how improbable, fix it.

An older heuristic, often used for simpler products, is: "If it ain't broke, don't fix it"—a strategy demonstrably not competitive for large-scale, complex products. It is not competitive primarily because an element "good enough" in a small system is unlikely to be good enough in a more complex one. (As more and more parts are added, the system reliability will go down unless the individual part reliabilities go up.)

The practical value of heuristic insights is seen in their extensions by W. Edwards Deming, Joseph M. Juran, Genichi Taguchi, and others. These are known as total quality management (TQM), continuous measurable improvement (CMI), just-in-time (JIT) inventories, and other techniques.

A quite different heuristic, useful in aerospace and computer design, is: "In partitioning a system into subsystems, choose a configuration with minimal communications between the subsystems." With a few word changes, this could be applied to the design of communication networks, organizations, and system subcontracts.

Example: A common question in the design of complex, smart spacecraft is whether to use a centralized or distributed computer system to run the major subsystems, such as propulsion, guidance, control, command, telemetering, science instrumentation, and system test. The centralized configuration is generally lighter, smaller, computationally more efficient, and less power consuming. The distributed configuration requires less information transfer, and solves local problems locally. But most important, it permits each subsystem to be self-testing without recourse to a central control unit. As such, it enables subsystem subcontractors to deliver checked-out units to a prime contractor. To do likewise, a centralized configuration requires central computer copies at each subcontractor site and/or delivery of subsystems that can be checked out only at the system level—a contracting nightmare and a prescription for overruns and delays. Fixing such problems usually requires adding weight, space, power, and computer capacity late in the development. The decentralized configuration is now preferred, for management and not technical reasons.

Heuristics cannot promise that a heuristically designed system will be the best performing of all possible systems. But, from experience, that type of system will be much

Teaching systems architecting: science and art

Instructing others in systems architecting involves both its science and its art. Teaching the underlying science is straightforward; teaching the art is still in the experimental stage. Existing guidelines are few, even from classical architecture.

What does seem to be true, though, is that until the science of systems architecting is understood and the complexities of systems experienced, the role of its art is little appreciated. Consequently, at the University of Southern California (USC) in Los Angeles, systems architecting is taught only to engineers with three or more years of experience (the average is seven years)—those who already recognize that the science of engineering, though powerful indeed, is somehow not sufficient to meet the demands they face in building complex systems.

The challenge is to teach the art without crushing its creative core under a burden of memorized dictates and caveats.

CODIFYING COMMON SENSE. Fortunately and perhaps surprisingly, codifying the common sense of successful systems architects is not so difficult. The first step is to show students that what is meant by common sense is contextual sense: what seems sensible depends on the system's particular context (whether the system is a building, an aircraft, a spacecraft, a missile, a computer, software, a network, or an organization).

That means that a heuristic (an empirical rule of thumb) that applies in one context may not apply in another. True, a heuristic that is sensible in one context may be sensible in another, but showing applicability has to be by example to be credible. It cannot be deduced mathematically. Instead, a proposed heuristic, on presentation to people versed in a field, has to seem "reasonable" to them and then must survive their almost automatic mental search for supporting or contradicting examples.

A diligent search for useful heuristics reveals a wealth of wisdom and lessons learned in many fields. Once given the concept of heuristics as architectural aids, an alert student can spot statements of common sense in most articles describing successful or unsuccessful systems.

At USC, well over 100 heuristics have been found or newly articulated for the acquisition of electrical and aerospace systems. Comparable numbers no doubt can be found scattered through the literature of computers, software, manned space flight, shipbuilding, law, economics, and management.

Though it might be wished that only a handful of heuristics existed that might be used as a checklist for all occasions, that does not seem to be the case. Different heuristics apply to the different phases of system acquisition—conceptualization, engineering, design, production, test, certification, and operations.

Basically, architecting is both multidimensional and relational; it has many parts, some of them related to several others. Its problems come in sets, not singly or in sequence. Similarly, its practitioners are multifaceted, broad-ranging, "renaissance" people. Like systems, they seem to have no bounds to their thinking and inquiry. If heuristics are to be taught, they have to be taught not as a bounded set of rules, but as a technique, an abbreviated form of experience and the starting point for creativity.

One technique of instruction might be the one commonly used for teaching law, economics, and conventional architecture: case studies. But the context of the system poses a practical difficulty. Doing a detailed case study of an aircraft system might not be of much help to a telecommunications architect and vice versa. Unless the heuristic fits the student's system and context, it will not be remembered when it counts. And in a typical USC class of graduate students—systems engineers from local aerospace and electronic firms—there may be as many systems of interest as there are students.

A CASE IN POINT. In the classes in systems architecting at USC, each student is asked to choose a system of personal interest, using it as a frame of reference to which the ideas in the course can be attached. Each student thus develops a personal case study as the course progresses. Although the technique works well, it does require that the student know at least one system in some detail. For the time being, at least, that confines it to the graduate level and for practicing engineers.

The hundred-plus heuristics studied so far range from the energy management system of the General Motors Corp.'s upcoming electric car to the U.S. government's Strategic Defense Initiative. And the insights the students have brought to the class—both their own and those of the architects they interviewed—have contributed substantially to the field of systems architecting.

Better yet, the students have been able to apply the lessons learned back on their jobs by assessing and modifying the systems studied. One fact about heuristics has become evident: whereas the science of architecting can be used by people of many skill levels, using its art effectively takes experience and judgment in context.

That result might have been expected; it is characteristic of any art. No one becomes a musician by studying mathematics or drawing, much as those three arts might be intertwined philosophically.

USC has now established a formal Master of Science degree in systems architecture and engineering. The utility of the program has been validated by the number of graduate students enrolling in it and by executive-level endorsement from major companies in southern California.

The program consists of systems architecting theory and practice complemented by analytic courses in each student's specialty, such as aerospace and mechanical systems, automation and control systems, communication and signal-processing systems, computer and information systems, and construction and manufacturing systems.

USC's experience in this field has demonstrated that the tools for the art of architecting systems can be taught, that they can be applied effectively, and that they will appreciably shorten the time needed for students to become professional systems architects. —*E.R.*

less likely to encounter unpleasant surprises down the road. More resilient to changes in its technical, budgetary, political, and competitive environment, it is more likely to be "good enough" (satisfactory) and less likely be "the best possible" (optimum)—if indeed ■ "best" or optimum exists at all.

Why might an optimum not exist? Two relevant heuristics tell why. First, "No complex system can be optimum to all parties concerned, nor all functions optimized." Secondly, "A system tightly optimized for ■ particular competitive situation is unlikely to be presented with that situation (the competition knows better than to do so!)."

CRADLE TO GRAVE. Architecting does not end with a first rough sketch, but continues through production into operation. In many systems that have been the architectural successes of this century, such as the Apollo moon project, the original architects were active for the entire project.

Lacking such architecting continuity, systems integrity would have been threatened, early consideration of likely events and problems down the road might not have occurred, controversies over system test and acceptance would have been exacerbated, and accountability for operations would have been diffused.

Direct participation by the architect is most critical during two phases of system building: conceptualization and certification. Two heuristics succinctly say why. For conceptualization: "All the serious mistakes are made in the first day." And for certification: "Regardless of what has gone before, the acceptance criteria determine what is actually built." The architect's role is in establishing acceptance criteria at the outset and certifying compliance with them at the end.

During the other phases—system engineering, detailed design, development, production, diagnosis, and operation—the architect is ■ monitor, advising the client on how well the system is conforming to plan at each stage, suggesting actions that would benefit the system as a whole, and helping the system accommodate to change.

COMPLEMENTING STRATEGIES. Architecting is an ongoing process—one that continues until the system is acquired. It is not just ■ front-end design-and-proposal effort tossed over the transom to the next group.

In this respect, architecting historically predates and affirms the principles of concurrent engineering, total quality management, continuous measurable improvement, and just-in-time inventory. Like architecting, those strategies also call for bringing together design, engineering, and production in the interest of better products and systems.

There are, nonetheless, notable differences between them and architecting. Compared with concurrent engineering, architecting is broader in its scope, covering higher-level system concepts and focusing less on detailed design. Also, its organizational structure of ■ small team contrasts with the collective style of concurrent engineering, and it places heavier emphasis on the certification (buy-off) process. On the other hand, concurrent engineering, which is valuable in making designers more aware of production problems, postulates an ongoing product line and generally puts to one side questions of concept, certification, public policy, and post-sale accountability.

> The success or failure of many civil and defense systems depends mainly on their architecture

Thus, concurrent engineering and architecting complement each other. They might even be combined. For example, the architect could act as the chairman of the concurrent-engineering group, maintaining overall systems integrity and balancing the conflicting demands of design, engineering, and production.

Quality management strategies such ■■ total quality management, continuous measurable improvement, and just-in-time inventory are based on normative rules for processes to make similar products with an established architecture. In contrast, architecting creates something new, an original effort for which data (and solutions deduced from the data) are unavailable, established procedures may be inadequate, and clients' needs are ill-formed, inconsistent, and conflicting—even into operation.

STAKES ARE HIGH. Staying up-to-date in systems architecting requires an awareness of ongoing research in the field. In today's competitive world, learning and teaching cannot remain static. Not only must individuals participate in lifelong learning, but instruction also must advance based on several promising areas of research:

- Techniques for assessing architectures, architecting, and architects prior to, during, and after system construction. Application: management.
- The behavioral and functional profiling of architects and architectural teams for creating effective architectures. Application: hiring personnel and forming compatible teams.
- The effects of the political process on system architecture and design; for example, changes in taxation, regulation, privatization, national security policy, and space exploration mission priorities. Application: government.
- The design of ultraquality systems whose failure rate is intended to be so low as to be statistically unmeasurable prior to use, as for spacecraft to the planets and for nuclear power plants. Application: product and process certification.
- The design of purposefully opposed systems, such as opposing weapons and cryptographic systems. Application: defense and security systems.
- Biologically inspired architectures for intelligent machines, such as neural networks, associative memories, and artificial intelligence languages. Application: designers of smart systems and their software.

All in all, the future of systems architecting and instruction in it is exceptionally promising. Technological developments and programs of national scope are increasing the need, which is felt by both individuals and companies.

TO PROBE FURTHER. Perhaps the first text to relate the process of architecting to that of systems and their engineering is *Systems Architecting: Creating and Building Complex Systems*, by Eberhardt Rechtin, published by Prentice Hall, Englewood Cliffs, N.J., 1991.

A classic book of heuristics—and satire—applicable to defense systems acquisition is *Augustine's Laws*, by Norman R. Augustine, published by the American Institute of Aeronautics and Astronautics, Washington, D.C., 1982.

A famous system architect-engineering text, applicable well beyond its own field, is *The Mythical Man-Month, Essays on Software Engineering*. by Frederick P. Brooks Jr., published by Addison-Wesley, Reading, Mass., 1982.

ACKNOWLEDGMENTS. The work reported here has been supported by the School of Engineering of the University of Southern California in Los Angeles, with encouragement and student tuition support from southern California aerospace companies, especially Aerospace Corp., Hughes Aircraft, the National Aeronautics and Space Administration/California Institute of Technology's Jet Propulsion Laboratory, Northrop, Rockwell International, and TRW. Key insights have been provided by Harry Hillaker, Gerald Nadler, Robert Spinrad, Albert D. Wheelon, and dozens of students.

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Rechtin has been an assistant director of the California Institute of Technology's Jet Propulsion Laboratory in Pasadena, a director of the Defense Advance Research Projects Agency, an assistant secretary of defense (telecommunications), and the chief engineer of Hewlett-Packard Co. He was the chief architect and director for the National Aeronautics and Space Administration of the Jet Propulsion Laboratory's Deep Space Network for its first 10 years of construction and use in tracking spacecraft. ●

Howard S. Jones, Jr.

This U.S. government engineer kept improving antenna design while becoming a generous mentor to younger engineers

Pssst. Howard S. Jones Jr. is kind of embarrassed about being profiled. He is confident but modest, believing that his many accomplishments, such as innovations in microwave engineering, are testament enough to a successful career in public service.

Fortunately, some of Jones's colleagues are not so reticent. They describe a prolific inventor, ■ pioneer of lightweight conformal antennas (evident in missiles like the Patriot and space vehicles like the Voyager), and a generous manager who inspired young engineers and scientists while continuing himself to churn out about ■ patent a year.

Jones took an unusual route to engineering. He showed no interest in the profession until late in college. As an African-American youth in the 1920s and '30s, he knew of no career role model. Nor did he have ■ crystal radio set, a common toy of would-be engineers at the time. Only the guidance from his parents and, in particular, the persistence of his mother, a beautician, led Jones to engineering.

Today, in semi-retirement after 37 years at the U.S. Army's Harry Diamond Laboratory (HDL), Adelphi, Md., ■ preeminent defense lab, especially from the 1950s to '70s, Jones finds himself in demand not only as a technical consultant but as ■ role model as well.

MICROWAVE MAN. Just ■ stone's throw from where his career began at the old National Bureau of Standards, Jones now lives in northwest Washington, D.C., in a high-rise apartment building. At his dining room table, he flipped through three thick loose-leaf notebooks that document his career and educational records—letters of praise from companies like Westinghouse and Raytheon, *Who's Who* citations, four major Army awards, and many other honors, including the IEEE Fellow grade and the Harry Diamond Award, presented by the IEEE Antennas and Propagation Society at its 1985 international symposium. This collection is factual evidence. As the baseball pitcher Dizzy Dean said: It's not boasting if you've already done it.

But not until he is asked to show his 31 patents, with their blue ribbons and gold seals, does the enthusiasm for which he is renowned burst through. Now, rather than talking about himself, he is discussing technology, specifically about his first solo U.S. patent, No. 3 029 430, "Antenna Testing Shield."

"This—I have to tell you something about this," he began excitedly, as if he could not speak the words fast enough. "This was a way of testing ■ fuzing system where you put this hood over it and want to simulate free space. We had all sorts of problems getting it done." He ticks them off, electrical and mechanical, and concludes, with a big smile, "I think they're still using it today."

Chances are that if a radar is sleek and compact, like those on missiles and planes, it benefits from Jones's ideas. "He contributed a lot to making Army missile technology possible," said Arthur Sindoris, deputy director of signatures, sensors, and signal processing at the U.S. Army Research Laboratory, which is to absorb the Harry Diamond Lab this October. Jones designed most of the HDL's radar fuze antennas for the generations of Army missiles—for instance, Corporal, Hawk, Lance, Little John, Pershing, and Patriot.

> 'I try to look at things untraditionally'

He was also sought by the U.S. Air Force for some of its projects, including the classified Bomarc air-defense missile program of the 1950s. United States Air Force Lieutenant Colonel Laslie M. Stewart wrote, in ■ 1968 memo to the IEEE in support of Jones's Fellow nomination, to say that Jones had saved the service millions—over US $2 million on the Bomarc fuze antenna system, and almost another $0.5 million over contractor costs on another classified missile fuze antenna in 1960–61.

James Salerno, a former chief of the advanced research lab at HDL, noted Jones's pioneering work in phased arrays: "It's sort of unfortunate that the work was classified. It detracted a lot from the visibility he would have received."

Jones spent most of his career at the HDL, which was divested from the National Bureau of Standards in 1953. The HDL was a premier research institution during much of his time there. Industry ranked the lab No. 1 in the nation, according to an April 24, 1970, memo from the Pentagon's Office of the Director of Defense Research and Engineering.

A FOUNT. Early on, Jones was part of ■ lab team that explored troublesome details or things not foreseen in contracts—a common occurrence since "all new systems are based on dreams," said one ex-lab engineer.

Billy M. Horton, a pioneer in fluidics and HDL's technical director until 1974, called Jones "one of the best performers and leaders in the lab." He worked within strict aerodynamic parameters that limited the size, weight, volume, and electric properties of the antennas. "That's no easy trick to perform," Horton said. "If it was designed by a pure antenna man, it might look like an orange crate."

Jones himself said, "The restrictions were good. It was ■ challenge."

Probably his most important contribution, spread over a series of patents, was that of conformal antenna arrays—built first with waveguides, then with printed circuits. Previous missiles had protruding monopole or dipole antennas. Jones embedded copper within the skin of the missile to form its antenna [see the cylindrical missile cross section in the photo at right, taken at HDL's Patriot missile antenna lab]. Today, the idea is being used in the development of "smart skins" for U.S. fighter aircraft and is instrumental in increasing stealthiness.

A related contribution was Jones's idea for metallic depositions on plastic foam that enabled the development of especially lightweight antennas. Westinghouse Electric Corp., Pittsburgh, pursued Jones's work for the Air Force's Rome Air Development Center in New York State, and Raytheon Co.'s Missile Systems Division, Bedford, Mass., also developed this lightweight innovation.

His wide interests led Jones to such varied fields as materials, circuitry, and manufacturing—and from theory to systems integration—anything that could improve the cost, performance, and quality of antennas.

Keith R. Carver, dean of engineering at the University of Massachusetts, Amherst,

John A. Adam Senior Associate Editor

Jim Pickerell

0018-9235/92/$3.00©1992 IEEE

Vital statistics

Name: Howard St. Claire Jones Jr.
Date of birth: Aug. 18, 1921
Place of birth: Richmond, Va.
Height, Weight: 180 cm, 82 kg
Family: wife, Evelyn Saunders Jones
Education: B.S. mathematics/physics, 1943, and D.Sc. (Honorary), 1971, Virginia Union University; MSEE, Bucknell University, 1973
Patents: 31
Favorite show: "Murder, She Wrote"
Management credo: "Interaction helps one's growth and understanding."
Mentors or strong supporters: Maurice Apstein, Jacob Rabinow, Robert D. Hatcher, and James Salerno, all of the U.S. Army Harry Diamond Laboratory
Professional engineering licenses: District of Columbia, Maryland, and Virginia
Motto: From his mother: "Never look back. Always look ahead and try to improve things."
Memberships: Fellow, the IEEE; Fellow, American Association for the Advancement of Science; Fellow, Washington Academy of Science; and Member, American Society for Engineering Education
Favorite award: IEEE Harry Diamond Award
Leisure activities: travel, jogging, tennis, golf

said that rather than focus on a tiny corner, Jones had the rare ability to "see ■ general problem and find ■ general answer." With his broad range of experience and contacts, he was able to work through problems and somehow come up with some clever ideas.

Sindoris, whom Jones recruited as a Ph.D. graduate from New York University in 1971, recalled that his boss would "probably file a patent or two ■ year. The rest of us were lucky if we could file one every couple of years."

Jones said, "I try to look at things differently, untraditionally. All the ideas I've come up with are ■ combination of university and industry interactions. You find out what they are doing, and often right away you can figure out improvements."

"I didn't do a whole lot on my own, but mainly put together ideas in ■ way that was meaningful," he admitted. He especially cites his role in evaluating industry's independent R&D programs (where companies would get ■ small percentage of a Government contract to invest in research of their own choosing). He was able to discover the problems, solve them, and sometimes spawn a new idea.

Throughout his career, Jones shared his technical know-how with small businesses. For instance, he passed on his expertise in building anechoic chambers and in casting waveguides. He also transferred lab technology to other Federal agencies, such as the Federal Aviation Administration and the Navy.

In his work, Jones liked to immerse himself in hardware. In his office was a large table covered with antenna models and, "during conversations, he'd jump up, bring over ■ model, and explain why it worked; and he'd probably pull two or three more out to compare," recalled Daniel Schaubert, a former HDL subordinate now at the University of Massachusetts. Jones also created "the museum," a showcase (and required tour) of the branch's achievements.

Salerno called Jones "an inspiring leader," who brought his group into diverse areas of activity as head of the microwave branch.

As a manager, Jones would use ■ "coaching style," Sindoris said. He led by example and helped people when they needed it, but he realized he could leave self-motivated professionals alone for a few days while he pursued his own technical work. He declined higher management positions in the U.S. government because he liked to have a foot in the laboratory.

ORIGINS. Jones grew up in Richmond, Va., with his parents and two older sisters. After graduation from high school, he worked at various odd jobs for ■ year and took ■ Federal exam for the postal service because he figured it would be a secure lifetime position. But his mother, "a very strong individual," insisted that her son attend college. She and Howard Sr. had been saving for his education. The postal job would always be there, she argued; she wanted her son to have other options. "Back in those days, you did what your parents wanted you to do," Jones said.

At Virginia Union University, a historically black college in Richmond, Jones discovered an aptitude in mathematics and physics and heard some professors talking about ■ profession called engineering. Their talks intrigued him, and after graduation, he made a big decision. "I had the undergraduate degree behind me and [I realized] I just wanted to be an engineer," he said. It was in the middle of World War II.

He moved to Washington, D.C., to accept a job as ■ junior engineering aide at the National Bureau of Standards (now the National Institute of Standards and Technology). While there, he took night courses at ■ Government school and at Howard University, also in Washington. "The Government needed engineers badly and had accelerated programs for people with science backgrounds," he said. "It really turned things around for me."

> 'I just wanted to be an engineer'

But the war also took him away from the NBS. The Army Quartermaster Corps called Jones to Fort Devens, Mass., where he taught basic science and metals' identification to ■ segregated unit. In June 1945 he went to Okinawa as a Signal Corps specialist and directed a field depot that examined enemy radar units from Japan. After 14 months, he declined offers to become an officer.

Instead he returned to the National Bureau of Standards. After passing the examination for permanent status as a P-1 physicist, he chose microwave engineering rather than electronic circuitry ■ his career focus.

The NBS itself was altered by the war. One of its researchers, Harry Diamond, had been working with weather balloon instrumentation when the British put in an urgent war request—they needed a proximity fuze to boost the damage of their bombs. The Diamond Ordnance Fuze Laboratory was formed. After the war, the lab's work was continued, and Jones joined the staff. "It was an awesome responsibility," Jones recalled. "All the services needed antennas for the fuzes."

Jones said he was never hampered much by discrimination, though he once declined a trip to Huntsville, Ala., during the segregated 1950s. Still, even in Government, he made it a practice to accumulate and record quantifiable achievements such as technical reports, conference invitations, and patents. "I didn't ever have to convince someone whether I was worthy of promotion," he said. "I had documentation." Still, Jones likes to point to the positive side. "You can do a lot to help it by displaying your ability and achievements," he noted.

CONSUMMATE PROFESSIONAL. Former HDL employees note (without even being asked) that Jones instilled a sense of professionalism in them. An aspect was that "you weren't a full professional unless you were active in ■ professional association," said the Army lab's Sindoris. True enough, many of Jones's recruits became active in the microwave or antenna societies of the IEEE.

The University of Massachusetts' Schaubert, who worked for Jones following his Ph.D. from the University of Illinois, Urbana, in 1974, said his former boss "really took an interest in our careers." He would take young inexperienced people and devote ■ lot of his energy to train them, whereupon they became so valuable and competent many other avenues opened up to them. "But Howard recognized even though it was a personal sacrifice to him, it was ■ contribution to the profession," Schaubert said.

Jones also takes ■■ active role encouraging students. Carver, the engineering dean, never worked for Jones but recalls a lecture by him when he was at New Mexico State University in Las Cruces in the early 1970s, near White Sands Missile Range. As usual, Jones brought ■ leather satchel of props, examples of his group's hardware. "You don't get too many who really show you how to do it, all the nuts and bolts, and with such enthusiasm," Carver recalled.

Jones has periodically taught at Howard University and lectured all over the country—from the Georgia Institute of Technology to the University of Maine and California State University to Ohio State University. He tells students that "engineering isn't always sitting down at ■ desk. You have to go into labs, machine shops, plating shops—all kinds of places and meet with different types of people."

"We don't do enough selling [of engineering] to encourage these students," Jones said, especially the women who, he has found, are often exceptionally bright and highly motivated. "We have to sell these students that there are jobs out here and these careers are interesting," he said.

In his semi-retirement, Jones has been called upon by the Army and the Strategic Defense Initiative Organization to work with some 70 colleges and universities, and to encourage minority students to pursue engineering and science.

Jones's colleagues in microwaves and antennas can admire his pioneering work. But his mother never could appreciate his full accomplishments. "She used to say, 'This is fine but you should come back [here] to teach.' "

The U.S. government and the engineering profession can be grateful that, this time, Jones did not heed her advice. ◆

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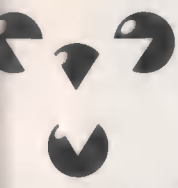

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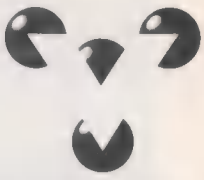

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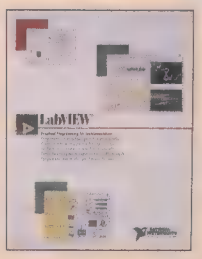
Software reviews

Virtual instruments

by Ken Johnson

LabVIEW for Windows, Version 2.5. *National Instruments Corp. A software system for creating and using virtual instruments requires an IBM 386-based PC or or compatible with 387 coprocessor. US $1995.*



LabVIEW for Windows (LVW) Version 2.5 does an excellent job of bringing an icon-based programming environment for developing virtual instruments [*IEEE Spectrum*, August 1990, pp. 36–39] from the Macintosh to the PC. Starting with the install program, which ran without a hitch, just about everything in this package worked flawlessly.

LVW's tutorial indicates that the right mouse button accesses a set of dialog menus. By selecting "file operations" and the OPEN command, a dialogue box pops up that lets a user select the virtual instrument (VI) libraries. The tutorial next instructs the operator to select a VI called "temperature system," which it then retrieves to show an instrument front panel.

The tutorial next instructs the operator to look at the diagram of the VI used for the temperature system and explains the functions and wiring capabilities of the icons. Wires can be dotted lines (to represent boolean, true, or false data), solid lines (indicating numeric data), or heavy lines (indicating bundled data).

Icons within the VIs may contain sub-icons, which may also contain sub-icons. This nesting provides a well-organized hierarchy. I did not find any limit on the number of hierarchical levels in the documentation; nor was I prevented from creating a hierarchy by some functional limit.

After getting used to some of the available functions, creating the VIs was simple. . . and actually fun. To create a measurement function, one first builds a functional instrument front panel.

To build the front panel, a user alternates between a panel window and a wiring-diagram window. In the panel window are graphics representing items such as switches, lamps, displays, and indicators. The wiring-diagram window contains the items from the panel in functional blocks, wiring to interconnect the front panel switches and lights, and the communication elements needed to interact with the instrument hardware. In addition, there is a set of logical operators and constants that can be "wired" into the circuit.

Since this was a beta version of the software, it was not surprising that straying from the defaults could cause the system to hiccup at times; this was especially true in selecting fonts, type sizes, and other inconsequential items. But no matter what I did, I was pleased to find that LVW would not crash and dump me back into DOS.

One of the VIs I was able to build and use was a spectrum analyzer made using an HP 8903A Distortion Analyzer. Though the HP instrument slowed it down, the function worked well. Since it was a fairly complex function, the PC bus was monitored for activity related to instrument handshake-control lines. The monitoring showed that the VI software was responsive, not allowing more than one bus cycle between the release of the bus and the next operation.

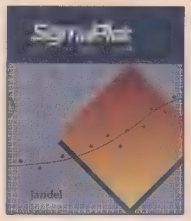
Another trial VI was based on a VXI 5-1/2-digit multimeter (HP E1411) connected to test points by an VXI crosspoint switch (HP E1466); both instruments were controlled by a VXI command module (HP E1405). Experimentation again showed that the software operated faster than the hardware; an actual test stand built using LVW would only have to wait for the hardware to settle, not for the software. *Contact: National Instruments Corp., 6504 Bridge Point Parkway, Austin, Texas 78730-5039; 512-794-0100; or* **circle 106.**

Ken Johnson is president of Testech Ltd., Oswego, Ill.

3-D graphs and more

by Brett D. DePaola

SigmaPlot 5.0. *Jandel Scientific. A PC-based system for generating two- and three-dimensional scientific graphs. It requires a minimum of a 286-based IBM PC or compatible with 640K bytes of RAM. DOS 2.0 or higher. US $495.*



With version 5.0 of SigmaPlot, Jandel has integrated a long-awaited three-dimensional graphing package into its already superb two-dimensional system. The platform used to evaluate the latest version was a 24-MHz, 386-based PC; the average access time for its hard disk was 26 ms. Although the package comes with drivers for virtually any hard-copy device, monitor system, and pointing device one can imagine, it was very easy to install. The tutorial is informative and easy to follow.

The beauty of SigmaPlot is its blend of ease of use and total control. It works like this: SigmaPlot produces a plot with convenient defaults (auto-scaled x, y, and z range, tic size, symbol size and type, line type, and so forth), which may then be easily modified if desired.

Besides ease of plotting, another beneficial feature of SigmaPlot is contained in the Math submenu. Here, one can create or manipulate data with built-in or user-supplied functions. One can also do very sophisticated nonlinear least-squares curve fitting. Because the 3-D routines of version 5.0 are integrated with the basic 2-D package, users of SigmaPlot 4.x will very quickly come up to speed in making 3-D graphs.

The only negative aspect of SigmaPlot 5.0 is that, with all the overlays it uses, it is terribly slow. Since the delay is due to disk access, a faster processor does not help. (The manual does give information on how to use extended memory as a cache to speed up the program, but I did not have the available memory to test this out.) With the exception of the speed problem, SigmaPlot is a wonderful package; I cannot imagine using anything else for producing scientific plots. *Contact: Jandel Scientific, 65 Koch Rd., Corte Madera, Calif. 94925; 415-924-8640; or* **circle 107.**

Brett D. DePaola is professor of physics in the department of physics at Kansas State University in Manhattan, Kan.

COORDINATOR: Gadi Kaplan

Recent software

RAVE version 1.4. A multimedia development tool and run-time package for 386- and 486-based PC systems. US $750, with 90-day Hotline support. *Contact: Microware Systems Corp., 1900 N.W. 114th St., Des Moines, Iowa 50325; 515-224-1929; or* **circle 108.**

NetShield 1.0. A NetWare loadable module for servers using Novell NetWare 3.1 that scans files for viruses. US $495 up per server; a license for corporate-wide, unlimited use is available for $30 000. *Contact: McAfee Associates, 3350 Scott Blvd., Building 14, Santa Clara, Calif. 95054-3107; 408-988-3832; or* **circle 109.**

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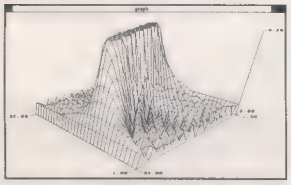

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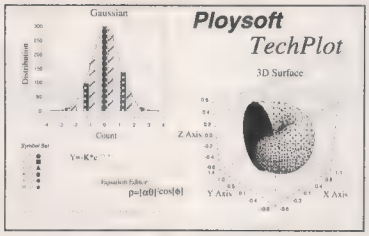

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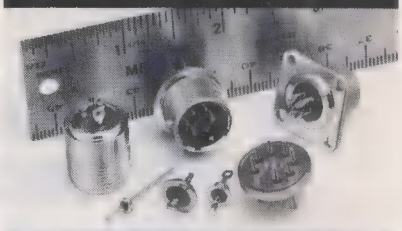

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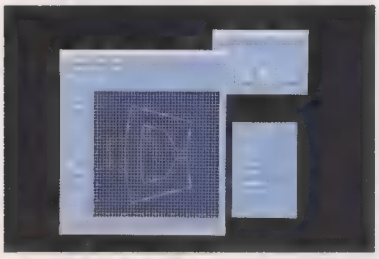

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Calendar

(Continued from p. 18D)

Sasaki, Department of Electrical and Computer Engineering, Engineering Science Building, University of Texas at Austin, Austin, Texas 78712-1084; 512-471-6734.

International Conference on Wafer Scale Integration (C, CHMT); Jan. 20–22; Fairmont Hotel, San Francisco, Calif.; R. Mike Lea, Brunel University, Uxbridge, England UB8 3PH; (44+895) 203 221; fax, (44+895) 258 728.

Annual Reliability and Maintainability Symposium (RAMS) (R); Jan. 26–28; Westin Peachtree Hotel, Atlanta, Ga.; V.R. Monshaw, Consulting Services, 1768 Lark Lane, Cherry Hill, N.J. 08003; 609-428-2342.

Power Engineering Society Winter Meeting (PE); Jan. 31–Feb. 5; Hyatt Regency Hotel, Columbus, Ohio; T.C. Wong, American Electric Power Service Co., One Riverside Plaza, Columbus, Ohio 43215; 614-223-2235; fax, 614-223-2205.

FEBRUARY

Workshop on VLSI (C); Feb. 7–10; Asilomar Conference Center, Monterey, Calif.; IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903; 202-371-1013; fax, 202-728-0884.

International Solid-State Circuits Conference (SSC et al.); Feb. 24–26; San Francisco Marriott Hotel, San Francisco; Diane S. Suiters, 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-639-4255.

MARCH

Multi-Chip Module Conference (ED); March 16–19; Cocoanut Grove, Santa Cruz, Calif.; S. Simon Wong, CIS-202, Stanford University, Stanford, Calif. 94305-4070; 415-725-3706; fax, 415-725-6949.

International Reliability Physics Symposium (ED); March 21–25; Hyatt Regency Hotel, Atlanta, Ga.; David A. Baglee, 5604 Cometa Court N.E., Albuquerque, N.M. 87111; 505-893-3446; fax, 505-893-1049.

International Conference on Microelectronic Test Structures (ED); March 22–25; Gran Sitges Hotel, Barcelona, Spain; Loren W. Linholm, National Institute of Standards and Technology, B360 Technology Building, Gaithersburg, Md. 20899; 301-975-2052; fax, 301-948-4081.

MAY

Custom Integrated Circuits Conference (ED); May 9–12; Town and Country Hotel, San Diego, Calif.; Roberta Kaspar, 1597 Ridge Rd. West, Suite 101C, Rochester, N.Y. 14615; 716-865-7164; fax, 716-865-2639.

Photovoltaic Specialists Conference (ED); May 10–14; Galt House, Louisville, Ky.; Eldon C. Boes, National Renewable Energy Laboratory, Suite 710, 409 12th St., S.W., Washington, D.C. 20024; 202-484-1090; fax, 202-484-8177.

International Symposium on Power Semiconductor Devices and ICs (ED); May 17–19; Hyatt Regency Monterey Hotel, Monterey, Calif.; M. Ayman Shibib, AT&T Bell Laboratories, Box 13566, Reading, Pa. 19612-3566; 215-939-6576; fax, 215-939-6795.

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The Art of Recording: The Creative Resources of Music Production and Audio. *Moylan, William,* Van Nostrand Reinhold, New York, 1992, 260 pp., $39.95.

The VAX Book: An Introduction. *Hubbard, J.R.,* McGraw-Hill, New York, 1992, 340 pp., $22.95.

Microsoft Word For Windows Step by Step, Version 2. *Microsoft Press,* Microsoft Corp., Redmond, Wash., 1992, 296 pp., $29.95.

Electronic Components: A Complete Reference for Project Builders. *Horn, Delton T.,* TAB/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 315 pp., $18.95.

The Mind Of God: The Scientific Basis for a Rational World. *Davies, Paul,* Simon & Schuster, New York, 1992, 254 pp., $22.

The Relational Database Advisor: Elements of PC Database Design. *Saunders, Kimberly Maughan,* Windcrest/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 221 pp., $16.95.

UNIX System V Commands: Programmer's Rapid Reference. *Peterson, Baird,* Van Nostrand Reinhold, New York, 1992, 137 pp., $29.95.

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Complete Guide to Microsoft Excel Macros. *Kyd, Charles W.,* and *Kinata, Chris,* Microsoft Press, Redmond, Wash., 1992, 512 pp., $29.95.

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Disaster Recovery Planning: Networks, Telecommunications, and Data Communications. *Bates, Regis J. (''Bud''),* McGraw-Hill, New York, 1992, 157 pp., $34.95.

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Supercharged C++ Graphics. *Adams, Lee,* Windcrest/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 487 pp., $24.95.

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Multimedia Applications Development: Using DVI Technology. *Bunzel, Mark J.,* and *Morris, Sandra K.,* McGraw-Hill, New York, 1992, 264 pp., $39.95.

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Maintain & Repair Your Computer Printer and Save a Bundle. *Bigelow, Stephen J.,* Windcrest/McGraw-Hill, Blue Ridge Summit, Pa., 1992, 228 pp., $16.95.

Forum

(Continued from p. 6)

serting the necessary coins (or paper money). The machine returns the ticket to you, and you insert it in a slot at the exit gate. The machines will also make change and even—in some cases—give you a receipt if you wish.

Look also at their small (maybe 0.45 meter to 0.60 meter) satellite dishes, which have been in use there for at least five years. The French and Germans even have ■ low-tech system that impels the shopper to return shopping carts to the right place.

Richard H. Engelmann
Cincinnati, Ohio

Improving on police radar may best occur by reviewing a 50-year-old design. As early as World War II, a few IRE engineers, using strong magnets, proved that one single frequency of electromagnetic radiation, which includes visible light, could travel faster than the speed of light, or 300 000 kilometers per second. A moving target indicator (MTI) radar outputs essentially one frequency from ■ magnetron. It receives back many different frequencies, depending on the radial velocity of the many possible targets. All closing targets send back ■ higher frequency than was transmitted. Opening targets send back a lower frequency.

John W. Ecklin
Alexandria, Va.

CASE note

As vice president of technical services for ATA Inc., I believe that Capers Jones in his article "CASE's missing elements" [June, pp. 38–41] mistakenly asserts that "the concept of templates for standard document types is missing from CASE [computer-aided software engineering] tool suites."

Cadre Technologies (the developers of Team*work*) has been offering document templates for DOD-STD-2167 (and later revisions) since 1987. These templates have been developed by ATA specifically for Cadre. IDE (the developers of Software Through Pictures) has also been offering the templates since 1988.

Currently, ATA offers DocEXPRESS, an automated document generation tool for DOD-STD-2167A, DOD-STD-1703, and DOD-STD-7935A, as well as others. The tool produces documents in both Interleaf and FrameMaker formats complete with automatically generated hypertext links to objects within the CASE tools repository. Additionally, ATA offers document templates for the above standards in Interleaf and FrameMaker formats (ATA/Templates), as well as templates for CASE tools and other add-on products for CASE tools.

Larry Stein
Torrance, Calif.

Corrections

On p. 3 of the July issue, the second sentence under May 27 should have read: "The combined group will retain the Sprint name and will be the only leading U.S. carrier to operate in three major telecommunications markets: long distance, local service, and cellular communications."

On p. 35, in the middle of the first full paragraph in the left column, the correct spelling of the name is Hideyuki Takagi.

On p. 55, the name in the first line of the third paragraph of the first column should have been Alan V. Oppenheim. —*Ed.*

Readers are invited to comment in this department on material previously published in *IEEE Spectrum*; on the policies and operations of the IEEE; and on technical, economic, or social matters of interest to the electrical and electronics engineering profession. Short, concise letters are preferred. The Editor reserves the right to limit debate on controversial issues. Contacts: Forum, *IEEE Spectrum*, 345 E. 47th St., New York, N.Y. 10017, U.S.A.; fax, 212-705-7453. The Compmail address is ieeespectrum.

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Getting up to speed on concurrent engineering

To expand awareness about concurrent engineering in the United Kingdom, the Technical Information Unit of the Institution of Electrical Engineers (IEE) has put together what it calls an information pack on the subject. The 111-page volume, which was compiled by Chief Information Officer John Coupland, includes summaries of technical papers gleaned from the world technical press, a short list of books and conference proceedings, and descriptions of more than two dozen software programs.

The book has chapters that give details on UK-based computer consultancies that specialize in manufacturing. And it lists training courses given in that country. The concurrent engineering information pack sells for £37 (US $74). *Contact: Publications Sales, IEE, Box 96, Stevenage, Herts. SG1 2SD, United Kingdom; (44+438) 313 311; fax, (44+438) 742 792; or* **circle 101.**

SOCIOTECHNOLOGY

Nonpolluting component cooler

A well-established technique for identifying defective components, bad solder joints, and hairline cracks in printed-circuit boards is to spot-cool them with a refrigerant spray. Unfortunately, the traditional cooling spray materials—chlorinated fluorocarbons—are serious environmental pollutants, which attack the ozone layer. The nonessential release of these materials has therefore been banned by the Federal government, and their production will be prohibited completely after Dec. 31, 1995.

A superior and much cheaper means for spot-cooling components is the COMP-CO_2LD component cooler, which uses common recycled carbon dioxide to push temperatures as low as –75 °C (compared with around –30 °C for a typical canned fluorocarbon spray). The COMP-CO_2LD's spray pattern is easily adjustable, so the coolant may be directed only where it is wanted. Because of its much lower temperature limit, the COMP-CO_2LD works more quickly than canned fluorocarbon sprays, and uses less refrigerant into the bargain.

Speaking of bargains, carbon dioxide sells for about US $1 per kilogram (that is to say, it costs less than $10 to get a 20-pound cylinder refilled just about anywhere in the United States), compared with about $20/kg for canned fluorocarbon sprays. Like the fluorocarbons, CO_2 is a nonconductor and may be sprayed on live circuitry.

The COMP-CO_2LD is shipped assembled with a 2-meter hose terminating in a standard CO_2 bottle adapter. It is priced at $350. According to experiments and calculations carried out by Va-Tran, the device will pay for itself if it replaces as few as twenty-nine 0.6-kg aerosol cans. *Contact: Va-Tran Systems, 677 Anita St., Suite A, Chula Vista, Calif. 91911-4661; 619-423-4555; fax, 619-423-4604; or* **circle 102.**

Va-Tran Systems

COMPUTERS

Keyboard pairs sharing a computer

Have you ever worked on a computer-based project with another person and been frustrated by wanting to type your brilliant input while she was sitting at the keyboard? Or have you wanted to demonstrate a program to someone else and wished that you could do it without having him or her breathing down your neck?

These and other related problems are solved by the Model 90 dual-user interface from H&R Technology. It buffers the video signal from an IBM-type PC for simultaneous display on two monitors and routes the inputs from two keyboards to the computer. With the Model 90, one user is designated as local and works close to the computer system unit. The other, remote, user may be located up to 15 meters away.

The keyboards can each gain control of the computer simply by being typed upon. To keep the two from interfering with each other, a time-out delay prevents the idle one from accessing the computer for a user-adjustable interval after the last keystroke on the active one.

The VGA version of the Model 90 lists for US $280. A version for EGA, CGA, and Hercules graphics adapters is priced $20 lower. *Contact: H&R Technology, 1506 Brookhollow Dr., Suite 106, Santa Ana, Calif. 92705; 714-641-6607; fax, 714-966-1770; or* **circle 103.**

SOLID STATE

Amplifier cross-reference plus

A 56-page guide from Analog Devices Inc. gives information on a wide variety of amplifiers. It includes a cross-reference table, which presents Analog Devices' equivalents for products from 16 other manufacturers.

Also included is a section of product selection trees, which divides the company's amplifiers into five families: high-speed, precision, low-power, low-noise, and instrumentation. Those families are then further subdivided by various performance characteristics to help the user select the best one for any given application.

The free guide also has sections on military amplifiers, ordering information, and sales offices. *Contact: Analog Devices Literature Center, 70 Shawmut Rd., Canton, Mass. 02021; fax, 617-821-4273; or* **circle 104.**

INSTRUMENTATION

Clamp-on unit measures ac and dc

Measuring the mixed (ac plus dc) currents in, say, an electric vehicle is no fun using ordinary metering techniques. It requires de-energizing the equipment and breaking a line to insert the meter, and then powering down again to remove the meter and restore the line when the measurement is finished. Conventional clamp-on ammeters are not much help since they respond only to ac.

The model CG100D Current Gun, on the other hand, clamps around conductors up to 19 mm in diameter and measures ac, dc, and mixed currents up to 200 A without interrupting the circuit under test. The single-range pistol-shaped instrument has a 3-1/2-digit liquid-crystal readout on which it displays its measurements to the nearest 0.1 A.

The meter has a frequency range of dc to 1 kHz. For readings up to 100 A, it is accurate to within 1.5 A from 15 Hz to 100 Hz, and to within 3 A from 100 Hz to 1 kHz.

The CG100D has banana jack outputs that enable its measurements to be viewed on an oscilloscope or read on a voltmeter. It includes four AA cells, weighs 0.45 kg, and is priced at US $335. *Contact: Hub Material Co., 33 Springdale Ave., Canton, Mass. 02021; 617-821-1870; fax, 617-821-4133; or* **circle 105.**

COORDINATOR: Michael Riezenman
CONSULTANT: Paul A.T. Wolfgang, Boeing Defense & Space Group

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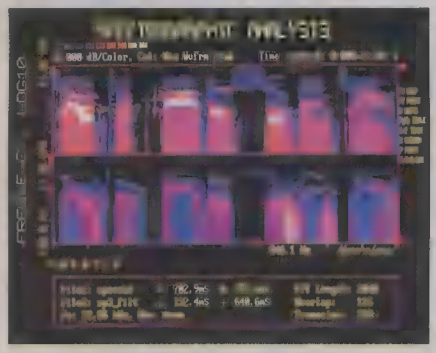

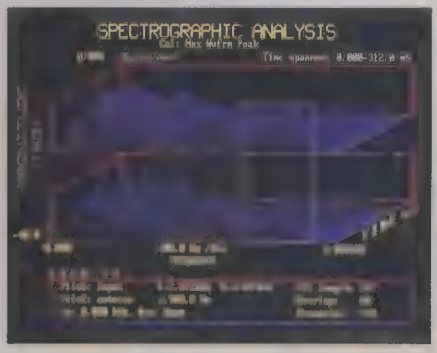

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CLASSIFIED EMPLOYMENT OPPORTUNITIES

The following listings of interest to IEEE members have been placed by educational, government, and industrial organizations as well as by individuals seeking positions. To respond, apply in writing to the address given or to the box number listed in care of *Spectrum* Magazine, Classified Employment Opportunities Department, 345 E. 47th St., New York, N.Y. 10017.

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IEEE encourages employers to offer salaries that are competitive, but occasionally a salary may be offered that is significantly below currently acceptable levels. In such cases the reader may wish to inquire of the employer whether extenuating circumstances apply.

Academic Positions Open

Tenure Track Faculty Position - University of Notre Dame - The Department of Electrical Engineering invites applications in the area of Electronic Materials. Special attention will be given to individuals specializing in materials growth or processing. Applicants should have a Ph.D. in Electrical Engineering, Materials Science and Engineering, or a related field. The Department offers B.S., M.S., and Ph.D. programs in Electrical Engineering and M.S. and Ph.D programs in Materials Science and Engineering. Active research areas include semiconductor materials and devices, materials characterization, device simulation, and high temperature superconductors. Applicants should have interest in teaching at the undergraduate and graduate levels, advising students, and conducting research. Rank and salary are negotiable. Interested persons should submit a complete resume and names of three references to: Dr. Daniel J. Costello, Chair, Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556. The University of Notre Dame is an Affirmative Action/Equal Opportunity Employer.

Director–The School of Electrical Engineering and Computer Science at Washington State University is soliciting applications and nominations for the position of Director of the School. The School presently has 39 full-time faculty, 452 undergraduates, and 171 graduate students. It awards B.S., M.S., and Ph.D. degrees in electrical engineering and computer science. Since 1985 the annual research budget has quintupled to $1.6 million. Major areas of research interest include energy systems, solid state electronics, communications and signal processing, electromagnetics, control theory, software engineering, graphics and visualization, and parallel computing. The School enjoys strong ties with local and national industries in a number of educational and research areas. Recently, the Boeing Company established the Boeing Centennial Chair in Computer Engineering, and the School has distinguished professorships in electromagnetics, analog electronics, and power engineering. In addition, an NSF Center for Design of Analog-Digital Integrated Circuits, with 15 industrial members and 3 affiliated universities, is based in the School. While our faculty represent diverse research interests, we also are united in our commitment to education. In recent years, several faculty members have been awarded NSF grants under the ILI Program and several have published textbooks. In the past year the industrial community has donated $3.1 million in state-of-the-art laboratory equipment and software to help maintain our tradition of "hands-on" education. Candidates must (1) possess a Ph.D. degree in electrical engineering, computer science, or a related discipline; (2) demonstrate outstanding leadership, an international research reputation, and a clear vision of the growth and development needed to enhance excellence in both teaching and research; (3) possess good communication skills and the ability to motivate people; (4) be able to interact productively with universities, industry, and government; (5) be committed to the promotion of faculty research activities and able to mentor junior faculty members to assist them in establishing strong research programs; (6) have a commitment to excellence in undergraduate education; and (7) be able to take the lead in the continued development of a diverse work force. Washington State University is a land grant university located in the beautiful rolling hills of Eastern Washington. The City of Pullman offers an ideal setting for family life; it has one of the best public school systems in the state, and recreational and outdoor activities are available year-round. The State of Washington has no income tax, real estate taxes are reasonable, and housing costs in the Pullman area are moderate. Applications and nominations should be sent to EECS Director Search Committee, School of Electrical Engineering and Computer Science, Washington State University, Pullman, WA 99164-2752. Screening of applicants will begin Nov. 1, 1992, and will continue until the position is filled. Washington State University is an equal opportunity/affirmative action employer. Members of ethnic minorities, women, Vietnam-era or disabled veterans, persons of disability and/or persons between the ages of 40 and 70 are encouraged to apply.

Chair in Photonic Systems. The Department of Electrical Engineering of McGill University is seeking an incumbent for a new Chair in Photonic Systems. Bell Northern Research and Northern Telecom Ltd., together with McGill University, will be seeking support for this Chair from the Natural Sciences and Engineering Research Council (NSERC) of Canada, through their Industrial Research Chair (IRC) program. Since this program is based on peer review, the successful candidate must be an internationally recognized authority, preferably working at the interface between photonic devices and systems, with outstanding scientific and leadership qualities that can bring the Department of Electrical Engineering to the forefront of research in Photonic Systems. An important condition for achieving this goal is the appointee's ability to build up a strong academic program for both graduate and undergraduate students. The position carries a highly competitive salary, junior faculty positions specifically designated in Photonic systems, necessary laboratory space and, above all, strong University support for the above stated goals. Interested candidates are invited to send their resume to: Professor N.C. Rumin, Chairman, Department of Electrical Engineering, McGill University, 3480 University St., Montreal, QC, Canada, H3A 2A7. McGill University is committed to equity in employment.

The University of Saskatchewan invites applications for a tenure track position in the Department of Electrical Engineering in the area of Power System Control. The responsibilities include teaching undergraduate courses in electrical engineering and power system control, graduate courses in power system control, and conducting research. Appointments are normally made at the Assistant Professor level. Applicant must hold an earned Ph.D. degree and have demonstrated potential for teaching at the undergraduate and graduate levels and for developing an independent research program. The department offers programs leading to B.E., M.Eng., M.Sc. and Ph.D. degrees. There are approximately 160 undergraduate and 90 graduate students in the department, and excellent research facilities. Curriculum vitae, a list of referees and a statement of research interests should be addressed to: M.S. Sachdev, Head, Department of Electrical Engineering, University of Saskatchewan, Saskatoon, Canada, S7N 0W0. Applications must be received by November 5, 1992. The expected appointment date is January 1, 1993. The University of Saskatchewan is committed to the principles of employment equity. Canadian citizens and permanent residents will receive first consideration. Applications of non-Canadians will then be considered.

Electronics & Telecommunications Research Institute (ETRI) of Korea seeks aggressive and dynamic individuals for both entry and senior level R/D positions to lead information and telecommunications science and technology towards 2000 and beyond. Ph.D.'s are preferred although experienced Masters are considered. All areas are open with primary needs in Communications Protocol, Digital System Design, Photonics, Optical Communications, Image & Signal Processing, System Control, Digital Switching, Multimedia Processing, Voice Code, Satellite & Mobile Communications, Microwave & Antenna, Software Engineering, Artificial Intelligence, Neural Network, Database, Computer Architecture, System Software, Semiconductor (VLSI, Materials, Devices, Design), Physical/Chemical/Mathematical/ Computational Sciences and Industrial/Systems Engineering. Physicists and scientists to do basic research are also sought. Salary is commensurate with qualifications and experiences. ETRI, founded and supported by the government, undertakes national research and development on advanced information technology. It aspires to become one of the world-wide leading R/D institutions by 2000. Applicants should send a resume, two references and statement describing past and future research and development interests to: Director, Human Resources Development Department, ETRI, 161 Kajung-Dong, Yousung-Ku, Daejeon, Republic of KOREA.

NSERC Industrial Chair in Applied Artificial Intelligence: Knowledge-Based Systems and Ebco/Epic Chair in Expert Systems - The Schools of Computing Science and Engineering Science in conjunction with the Centre for Systems Science at Simon Fraser University invite applications and nominations for these two Chairs at the senior Associate or Professor level. Applicants and nominees must have an outstanding research record, a commitment to teaching, and a demonstrated record of industrial collaboration. Background in an Engineering discipline would be an asset. The NSERC Industrial Chair in Applied Artificial Intelligence: Knowledge-Based Systems is intended for a specialist with ■ particular knowledge and experience with constraint logic programming approaches. This Chair is for an initial five year period during which time the primary responsibilities will be research and the training of graduate students. A five year extension is possible. The academic appointment will be tenured (or tenure-track if warranted). After the Industrial Chair position has expired, the individual will assume the responsibilities of ■ regular academic appointment. The Ebco/Epic Chair in Expert Systems is an endowed chair intended for a specialist in expert systems. This Chair is a continuing academic position affiliated with the Expert Systems Laboratory. The Expert Systems Laboratory is a joint university/industry laboratory founded in 1988 and sponsored by the B.C. Advanced Systems Institute to foster applied artificial intelligence research. The chairholders may participate in current projects and will be expected to participate in the development of future projects in the laboratory as well as in conjunction with industry. The NSERC Industrial Chair will be filled first and the successful applicant will participate in the selection of the Ebco/Epic Chair. Research funding is available as part of the Chair program. In accordance with Canadian immigration requirements, this advertisement is directed to Canadian citizens and Permanent Residents. Simon Fraser University is committed to the principle of equity in employment and offers equal employment opportunities to qualified applicants. Applications will be accepted until December 1, 1992. To apply, send a curriculum vitae, evidence of research productivity (selected reprints), and the

names, addresses and phone numbers of three referees to: Arthur L. Liestman, Director, School of Computing Science, Simon Fraser University, Burnaby, British Columbia, Canada V5A 1S6, Fax: (604) 291-3045.

Computer Engineering and Design, Control Systems and Design - The Department of Electrical Engineering of Western Michigan University invites applications for several anticipated tenure-track faculty positions at the Assistant/Associate/Full Professor levels. Preferred applicants must 1) have an earned PhD in Computer Engineering, Electrical Engineering, or the equivalent, 2) specialize in computer architecture, logic design, digital electronics and real-time embedded systems or in applied control systems, and 3) have industrial-level design experience. Responsibilities include graduate and undergraduate teaching, curricular leadership, and research. Senior faculty applicants should demonstrate experience in applied engineering design. Western Michigan University is located in Kalamazoo, Michigan and has approximately 26,000 students; it is one of the state's five graduate intensive universities and is designated a Carnegie Doctoral I university. The Department offers two EAC/ABET accredited undergraduate degrees (Computer Systems Engineering and Electrical Engineering) and a growing graduate program. We are especially looking for experienced computer engineers and control engineers who enjoy teaching and would like to participate in building a design-oriented graduate program in computer and systems engineering. Please send ■ detailed resume and the names of three references to: Dr. Thomas F. Piatkowski, Chair, Department of Electrical Engineering, Western Michigan University, Kalamazoo MI 49008-5006 or piatkowski@gw.wmich.edu. Applications will be accepted until the position is filled; we hope to fill some of the positions for January, 1993. Western Michigan University is an equal opportunity/affirmative action employer.

Stanford University: The Departments of Materials Science and Engineering and Electrical Engineering invite applications for a tenure track faculty position in the area of magnetic or optical information storage. A PhD and a strong interest in graduate and undergraduate teaching are required. The research activities of this individual should focus on the science and technology of information storage materials and devices and might embrace magnetic thin films, magneto optic materials, optical storage materials, or other relevant materials and techniques. The successful candidate will be embedded in an environment with substantial activities in surface and interface science, magnetism, solid state physics, advanced optics and nanostructure science and technology and have an interest in the fundamentals and applications of both materials and devices. The opening is at the Assistant Professor level. The appointment will be made either in the MS&E Department or the EE Department or both. Please send a complete resume, ■ publication list, a statement of research and teaching interests, and the names of three references to Professor Robert L. White, Department of Materials Science and Engineering, MS 2205, Stanford University, Stanford, CA 94305, by December 1, 1992. Stanford University is an equal opportunity/affirmative action employer and encourages applications from women and minority candidates.

Department of Computer Science - Faculty Positions - The Wayne State University Department of Computer Science invites applications and nominations for several anticipated, subject to budgetary approvals, tenure-track positions at all ranks. Candidates from all areas of specialization in computer science or computer engineering will be considered; however, the department will prefer candidates in the areas of expertise which overlap with the existing research strengths in computer graphics, virtual reality, modeling and data analysis, database systems, software engineering, artificial intelligence, computer vision and image processing, distributed systems and parallel high performance computing, neural networks, biocomputing, numerical methods and natural language processing. Candidates should have a Ph.D. in computer science/engineering or a closely related field, a strong interest in and commitment to both research and teaching, and demonstrated potential for obtaining external research funding. Applications from minority and women candidates are especially encouraged. Wayne State University, located in Detroit's Cultural Center, is an urban, comprehensive research university serving 34,000 students. The Department of Computer Science has sixteen faculty members, approximately 250 graduate students and 350 undergraduates. It offers the Ph.D., M.S., M.A., B.S., and B.A. degrees. The faculty have ties to industry (including local automotive and computer companies) and to several institutes for high technology associated with the University. Several research projects are currently being funded by NSF and NASA. Applicants should send a letter of intent, a statement of research and teaching interest, resume and names of at least three references, their addresses (including e-mail address) and telephone/fax numbers to: Dr. Narendra S. Goel, Chair, Department of Computer Science, Wayne State University, 431 State Hall, Detroit, MI 48202. Phone: (313) 577-2477. Fax: (313) 577-6868. E-Mail: ngoel@cs.wayne.edu. For full consideration, applications should be submitted by November 1, 1992. However, applications will be accepted until the positions are filled. Wayne State University is an Equal Opportunity/Affirmative Action Employer.

Research Associate - A university institute, dedicated to research in the applications of acoustics, is seeking a research associate to assist in laboratory work involving agricultural acoustics and ultrasonic nondestructive testing; to develop electronic instrumentation and interfacing with personal computers; and to analyze and display data in graphical form using personal computer systems. Requirements: Applicants should have a Master's degree in Electrical Engineering and three years experience in ultrasonic testing and acoustical engineering, and in the use of personal computer systems. Salary: $26,250.00 per year. Hours: 8:00 a.m. to 5:00 p.m., Monday - Friday. Closing date: October 31, 1992. Job Order Number (JON) M52620039. Contact: Mississippi Employment Services/EEO, 603 South Lamar, Oxford, Mississippi 38655.

The Air Force Flight Dynamics Laboratory and The Air Force Institute of Technology announce the 1993-1994 Flight Control Distinguished Visiting Professor Program - The Air Force Institute of Technology (AFIT) at Wright-Patterson Air Force Base, Dayton, Ohio announces the opportunity to join the AFIT graduate faculty as a Distinguished Visiting Professor of Flight Control in the Department of Electrical and Computer Engineering in the School of Engineering. Responsibilities - The responsibilities of the Flight Control Distinguished Visiting Professor include providing academic leadership in teaching and research in flight control, and initiating and conducting research and consultation with the Flight Dynamics Directorate, Air Force Wright Laboratory. Qualifications - The person appointed as Distinguished Visiting Professor should be an established faculty member at a major university. Prior flight control experience with industry or government would add to the candidate's qualifications. Areas of special interest for this chair are: Flight Control Systems, Control Systems for Reconfigurable Aircraft, Design of Robust Multivariable Control Systems, Quantitative Feedback Theory Design, Output Digital Feedback Design Technique for Multivariable Tracking Systems, and Adaptive Control and Estimation. Applicants are expected to have a Ph.D and documented contributions in the areas of flight control. Selection will be based on the candidate's experience and qualifications as well as on the proposed teaching and research program at AFIT. Research Support - Two powerful hybrid computers (EAI SIMSTARS) are the heart of AFIT's flight control laboratory. A high fidelity, full flight envelope, real-time aircraft simulator is developed for academic and research use. Overall, AFIT's computer resources equal or exceed those found at other universities. An office, laboratory, the use of modern computers, and other service support will be provided for the visiting professor and may include support for a limited number of the visiting professor's doctoral students. Period of Appointment and Salary - The initial period of appointment is for one full year. A shorter period and the starting date are negotiable, but should be prior to October 1, 1993. Salary is commensurate with qualifications. A per diem allowance is also paid. Application - A resume of qualifications and experience, including a list of significant publications in the above fields of flight control, and any need for support of Ph.D students can be submitted anytime prior to December 31, 1992 to: ASC/PKWRS (D. Peterson), Wright-Patterson AFB OH 45433-5000, Phone: (513) 257-6721. The Flight Control Distinguished Visiting Professor Program is made possible through a grant from the Air Force Wright Laboratory's Flight Dynamics Directorate. AFIT is an Equal Opportunity and Affirmative Action Employer.

University of Toronto - Department of Electrical Engineering - The Department of Electrical Engineering invites applications for a tenure-stream Assistant Professor position in the area of microelectronics. The applicant is expected to have a strong interest in both device and circuit design with an emphasis on high speed mixed analog/digital applications. The position involves both research and teaching at the undergraduate and graduate levels. Applicants must have a doctoral degree in Electrical Engineering, an outstanding academic record and effective teaching ability. The position is supported by Bell Northern Research/Northern Telecom Electronics with whom active interaction is expected. Additional research support may be available through the Natural Sciences and Engineering Research Council of Canada (NSERC) Research Partnership Program. Salary is commensurate with qualifications and experience. Applicants should send a curriculum vitae, a statement concerning teaching and research interests, and a list of three references before December 31, 1992 to: Professor Adel S. Sedra, Chair, Department of Electrical Engineering, University of Toronto, Toronto, Ontario M5S 1A4, Canada. In accordance with Canadian Immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada. The University of Toronto is committed to employment equity and encourages applications from women, visible minorities, aboriginal people and physically challenged persons.

University of Toronto - Department of Electrical Engineering - The Department of Electrical Engineering invites applications for two tenure-stream Assistant Professor positions in the area of Computer Engineering. The applicants are expected to have a strong background in the general area of computer systems. Subareas of specialization may include: systems software, computer architecture, and computer aided design. These positions involve both research and teaching at the undergraduate and graduate levels. Applicants must have a doctoral degree, an outstanding academic record and effective teaching ability. Salary is commensurate with qualifications and experience. These positions are two of several made possible by the expansion of the Department of Electrical Engineering and the establishment of a new undergraduate program in Computer Engineering. Applicants should send a curriculum vitae, a statement concerning teaching and research interests, and a list of three references before December 31, 1992 to: Professor A.S. Sedra, Chair, Department of Electrical Engineering, University of Toronto, Toronto, Ontario, Canada M5S 1A4. In accordance with Canadian Immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada. The University of Toronto is committed to employment equity and encourages applications from women, visible minorities, aboriginal people and physically challenged persons.

The University of Missouri-Columbia Department of Electrical and Computer Engineering invites applications for a visiting professor in the areas of computer engineering or computer science. This position is for the winter semester 1993 beginning January 1, 1993 and the fall 1993 semester ending December 31, 1993. Responsibilities include teaching undergraduate and graduate courses and student advising. Candidates must have an earned doctorate in Computer Engineering, Computer Science, or related discipline. Candidates should have an interest and background in artificial intelligence, neural networks, fuzzy logic, computer vision, or pattern recognition. Interested applicants should send a resume, a description of research inter-

ests and immigration status for non-United States citizens, as well as a description of research interests to: Jon Meese, Chairman, Department of Electrical and Computer Engineering, University of Missouri-Columbia, Columbia, MO 65211. The University of Missouri is an Affirmative Action/Equal Opportunity Employer.

Research Associate. The Department of Radiology at the University of Minnesota has an immediate opening for a research associate in Magnetic Resonance Imaging and Spectroscopy. A Ph.D. degree in physics or chemistry and experience in pulse sequence programming and design is required. The successful applicant will implement new pulse sequences on our clinical 1.5T Siemens SP 4000 scanners. The Radiology Department has a number of networked image processing workstations and provides access to supercomputer facilities. Research time is available on the Siemens whole body (125cm bore) 4.0T system and on small bore 4.7T, 5.0T and 9.4T animal research systems. Primary duties of the position will involve transfer of pulse sequences developed in a variety of federally and industrially funded research projects to the clinical domain. The position is currently available, and we will be accepting applications through November 30, 1992. The appointment is date specific and annually renewable, depending on performance and availability of funding. Salary is commensurate with experience. Prospective candidates should submit their curriculum vitae, three references and sample reprints to Dr. E.R. Ritenour, Department of Radiology, University of Minnesota, Box 292 UMHC, Minneapolis, MN 55455. The University of Minnesota is an equal opportunity employer and educator.

Northwestern University - The Robert R. McCormick School of Engineering and Applied Science - The Department of Electrical Engineering and Computer Science at Northwestern University has two tenure track faculty positions at the assistant professor levels in the areas of control systems and solid state devices. Outstanding candidates in other areas will also be considered. All candidates must have strong research and teaching capabilities. Northwestern University is an equal opportunity, affirmative action educator and employer. Applications from women and minorities are especially encouraged. Employment verifications required upon hire. Applicants should have attained a doctoral degree in electrical engineering or a closely related field by the starting date of the appointment. Interested persons should send their resumes and the names and addresses of at least four references to: Professor A.H. Haddad, Chairman, Department of EECS, Northwestern University, 2145 Sheridan Road, Evanston, Illinois 60208-3118 - (708) 491-3641.

Telecommunications: The University of Southwestern Louisiana (USL) is seeking applications for a senior engineering faculty member and a second tenure-track faculty position for their telecommunications program. The senior individual's primary mission is to develop the research stem of our new (Fall 91) graduate program. Both faculty members will be a part of USL's Center for Telecommunications Studies (CTS). CTS is the umbrella organization which coordinates the University's research, undergraduate, graduate and continuing education activities in telecommunications. The telecom option of the BSEE is an ABET accredited program that includes additional courses in the development of the industry and in management. It has graduated over 200 students since its inception in 1982. The current Telecom Option enrollment is 130 students out of 375 enrolled in the Electrical & Computer Engineering (EECE) Department. The MS in Telecommunications is an interdisciplinary program encompassing system engineering, system management and public policy. The University has submitted a letter of intent to offer a PhD in telecommunications to the Louisiana Board of Regents. USL also offers the MS and PhD in Computer Engineering and in Computer Science. The Department of Electrical and Computer Engineering has 14 full time faculty, 6 of whom are in telecommunications. The telecommunications laboratory has a digital switch for a small central office, two Local Area Networks for student experiments, two digital PBX's, two satellite modems for a simulated link, a terrestrial microwave link, and peripheral equipment. The university is well equipped with computers from networked PCs to workstations and an IBM 3090 with vector processor. Faculty divide their time between teaching, research and service to the profession as appropriate. The senior faculty member's duties will be primarily the development of our research program. Thus the individual should have an established record of research and publications. The other position is for a faculty member who will contribute to both the undergraduate and graduate programs. A strong relationship with industry is maintained through the INdustry Telecommunications Advisory Committee (INTAC). Current membership includes 37 individuals representing major corporations nationwide. To date the program has received over one million dollars in scholarships, equipment funds and grants. The state regulations require new engineering faculty to become registered Professional Engineers (PE) before tenure can be granted. Therefore, preference is given to PEs, EITs and those with ABET accredited degrees in addition to the PhD or equivalent. Salaries are commensurate with experience. One position is available in January 1993. We anticipate the senior position to be available for August of that year, pending budgetary approval. Applications will be accepted until the positions are filled. Apply to: Chairman, Faculty Search Committee, Electrical and Computer Engineering, University of Southwestern Louisiana, P.O. Box 43890, Lafayette, LA 70504-3890. 318/231-6568.

The Electrical and Computer Engineering Department at Illinois Institute of Technology invites applications for several tenure track positions. We have a strong preference for candidates in the areas of computers and telecommunications, but outstanding applicants in other areas will also be considered. Candidates should have an earned doctorate, demonstrated ability for independent research, and a strong commitment to undergraduate and graduate teaching. Applicants should send detailed curriculum vitae with names of three references to: Dr. Thomas Wong, Chair, Faculty Search Committee, Electrical & Computer Engineering Department, Illinois Institute of Technology, 3301 South Dearborn Street, Chicago, Illinois 60616. Illinois Institute of Technology is an equal opportunity, affirmative action employer, M/F/H/V.

Clarkson University, Electrical and Computer Engineering - Applications are invited for a tenure-track faculty position as Assistant Professor in computer engineering. Responsibilities include undergraduate and graduate teaching and development of a research program. Desired research areas include distributed and parallel computation, artificial intelligence, image and signal processing, neural networks, and robotics. A doctorate is required. Review of applications will begin on November 1st and will continue until the position is filled. The department, consisting of 23 faculty members, offers programs at the B.S., M.S., and Ph.D. levels. Last year 123 EE bachelors, 21 CE bachelors, 15 masters, and 2 doctorates were awarded, and research funding reached more than one million dollars. There are research labs in artificial intelligence and neural computing, VLSI design, and robotics and control. Clarkson is an independent university specializing in engineering, science and management with an enrollment of 3200 students, including 400 graduate students. Located in northern New York, Clarkson is close to Lake Placid and the Adirondack Mountains. Send applications to Professor Paul McGrath, Chairman, Department of Electrical and Computer Engineering, Clarkson University, Potsdam, New York 13699-5720. Clarkson is an Equal Opportunity/Affirmative Action Employer. Position No. 418.

Faculty Position - Clemson University: The Department of Electrical and Computer Engineering seeks candidates for one or more tenure track positions. Top priority will be given to individuals with a specific interest in the area of electronics design and the computer aided design of integrated circuits. It is anticipated that the successful candidate will have strong interest in applying computer aided design in one or more application areas in which the department is engaged—e.g. computer architecture, robotics, advanced communications systems, computer networking components, etc. Candidates should hold the Ph.D. degree in Electrical or Computer Engineering or Computer Science and have a strong interest in teaching at both the undergraduate and graduate levels. Clemson University's College of Engineering was listed as one of the United States' "up-and-coming" engineering graduate programs in the March 19, 1990 of the U.S. News and World Report. The ECE Department has 38 full-time faculty, approximately 500 undergraduate students, and 150 graduate students. It offers B.S., M.S., and Ph.D. degrees in both electrical engineering and computer engineering. Facilities include CAD laboratories using Mentor Graphics, Cadence/VALID Logic and a broad collection of public-domain tools hosted on a VAX 8810 and Sun and Digital Workstations. Clemson University is the land-grant university for South Carolina and is located in the state's scenic Piedmont region. The quality of life stems from the outdoor recreation available, the reasonable cost of housing and living, and the thriving metropolitan area of Greenville, approximately thirty miles from campus. Greenville is ranked by Inc. Magazine as one of the twenty fastest growing markets in the country. Interested persons should send a curriculum vitae and the names of at least three references to L. Wilson Pearson, Head, Department of Electrical and Computer Engineering, Clemson University, Clemson, South Carolina 29634-0915. Consideration of candidates will begin on November 1, 1992 and will continue until position(s) is (are) filled. Clemson University is an Equal Opportunity/Affirmative Action Employer.

Director - Oral & Maxillofacial Imaging Research Facility. A unique opportunity is available for a research faculty position immediately in the department of Dental Diagnostic Sciences. This position will be at either a professorial (tenure) track or scientist (non-tenure) track, depending upon qualifications and individual/program directions. Responsibilities of the successful applicant will include developing and directing research in the areas of image processing and image acquisition from both optical and x-ray sources. Research participation in an active and on-going program required. The individual must possess a PHD or have equivalent experience in image processing/acquisition. It is expected that the individual have an established record of grant submission and subsequent funding. Salary and rank commensurate with experience and qualifications. Indiana University is an Equal Opportunity/Affirmative Action Employer. Send Curriculum vitae and letters of recommendation to Dr. Steven L. Bricker, Chairman, Dental Diagnostic Sciences, 1121 W. Michigan St., Indianapolis, IN 46202-5186.

The Electrical Engineering Technology department at Purdue University announces anticipated academic-year, tenure-track positions at the assistant or associate professor level at West Lafayette, Anderson, Columbus, Kokomo, New Albany, and South Bend, Indiana, commencing during August, 1993. Major areas of study are: circuits, analog and digital electronics, microprocessors, industrial automation, power, communications, and telecommunications. Minimum faculty requirements are: a master's degree in electrical engineering, electrical engineering technology, or a closely related field; a minimum of three years of recent, relevant industrial experience; and a strong commitment to teaching. Applicants must have expertise in at least two specialty areas. Candidates from industry, engineering technology programs, or strong community college technical programs are encouraged to apply. In addition to teaching, faculty are expected to engage in curriculum development, perform some program coordination, do student advising, participate on committees at various levels, and pursue scholarly activ-

READER GUIDE TO PRODUCTS AND SERVICES

STUDENT EMPLOYMENT GUIDE

IEEE United States Activities has just published the second edition of the student version of *The Employment Guide for Engineers and Scientists*. In this two-volume publication, the first volume includes basic information on conducting a job search, writing a résumé, preparing for interviews, and developing a network to assist in the job search process.

The second volume is a *Directory of Employers of IEEE Members*, a state-by-state sourcebook that lists hundreds of companies, and includes telephone numbers and contact persons.

The book may be ordered through the IEEE Service Center (Order Number UH0188-3) for $14.95 for members and $19.95 for nonmembers, plus tax and shipping. Call 1-800-678-IEEE to order.

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- Optical Communications Technology and Systems
- Solid-state Laser Technology and Applications
- Optoelectronics Technology and Applications
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Being held along with LEOS '92 is a major trade show called OPTCON '92. OPTCON '92 is a jointly sponsored event addressing the needs of all professionals with an interest in optics and its applications: technicians, engineers, and pure and applied research scientists. The exhibition and core program are sponsored by the five major professional and trade associations with activities in optics, optical technology, applications of optics, laser technology, applications of lasers, and electro-optics.

For more information, contact IEEE/LEOS, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331; 908-562-3896; or CIRCLE #83 on the Reader Service Card.

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The 1991 IEEE U.S. Membership Salary and Fringe Benefit Survey price has been reduced by 50 percent. Members may now buy the survey for $37.50, nonmembers for $49.50. Included is information on salaries by geographic area, job function, level of responsibility, level of education, areas of technical competence, and several other parameters, as well as important fringe benefit statistics.

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CALL FOR PHOTOS

Visions of Technology: Powers of Energy Photography Contest

"Visions of Technology: Powers of Energy" is the theme of the 1993 National Engineers Week Photo Contest, sponsored by IEEE United States Activities. Practicing engineers and engineering students of all disciplines can tap their photographic talents to capture on film engineers' achievements as they develop and conserve our nation's energy resources. The powers of energy, whether solar, wind, water, electric, coal, nuclear, or human, are all germane to the theme. The only restriction is your imagination! Winners will be announced during National Engineers Week, February 14–20, 1993. Cash prizes of $500, $250, and $100 will be awarded.

DEADLINE
Entries must be postmarked by December 1, 1992.

FOR MORE INFORMATION:
Photo Contest, c/o IEEE-USA Office, 1828 L St., N.W., Washington, D.C. 20036-5104; 202-785-0017. Or CIRCLE #86 on the Reader Service Card.

PRESIDENTIAL CANDIDATES OUTLINE TECHNOLOGY POLICY AND COMPETITIVENESS PLANS

In statements to the IEEE, President George Bush and Governor Bill Clinton have outlined their plans for promoting U.S. economic competitiveness through technology policy. Their statements come in response to a challenge by IEEE President Merrill Buckley that they answer 10 key questions on the roles that the Federal government should play in this area. Buckley's call, made at an April 13 press conference in Washington, D.C., was intended to help raise the visibility of jobs, technology, and competitiveness as election year issues.

For a list of the 10 questions and copies of the Bush and Clinton responses, CIRCLE #87 on the Reader Service Card.

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ity by publishing and participating in professional society meetings. For priority consideration, applications should be submitted by January 15, 1993. The positions will remain open until filled. Send a detailed resume; the names, addresses and phone numbers of three references; and your location preference to: Chairman, Faculty Search Committee, Electrical Engineering Technology, Knoy Hall, Purdue University, West Lafayette, IN 47907-1415. Purdue is an equal opportunity/affirmative action employer.

University of Wisconsin-Madison - Faculty Associate Position - The Department of Electrical and Computer Engineering invites applications for a fixed term renewable academic-staff position. An M.S. degree in Electrical Engineering is required. Teaching experience is preferred. Responsible for teaching introductory undergraduate laboratories including lectures and videotaped presentations; developing new lab experiments; and training, supervising and guiding teaching assistants. Expected to also provide state-of-the-art engineering support and standards (including design and development) for intermediate and advanced undergraduate laboratories with input from faculty. Send resume by December 1, 1992 to Bahaa E.A. Saleh, Chairman, Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 1415 Johnson Drive, Madison, WI 53706, an equal opportunity/affirmative action employer. Names, titles and/or occupations, and addresses of applicants cannot be kept confidential.

The Department of Electrical and Computer Engineering at the University of the Pacific is accepting applications for a tenure-track position at the Assistant or Associate Professor level beginning September 1993. Candidates should have a Ph.D. with expertise in electronics; also some industrial experience is desirable. Undergraduate education is the primary responsibility; curriculum development, advising, MS-level teaching and clinic supervision, and scholarly activity/research are also expected. UOP is a private, comprehensive university with a total enrollment of approximately 3800 students. Send resume to: Dr. George Schroeder, Electrical and Computer Engineering, University of the Pacific, Stockton, CA 95211. UOP is an Equal Opportunity/Affirmative Action Employer.

University of Pittsburgh - The Department of Electrical Engineering invites applicants for tenure track faculty positions at the assistant/associate professor level beginning September 1993. Founded in 1787, Pitt is one of the oldest institutions of higher education in the United States. A strong, research oriented university with a commitment to high-quality education. Pitt is a long time member of the Association of American Universities (AAU), the prestige group of research universities. In our second century of educating electrical engineers, the EE Department consists of 28 faculty supervising 300 undergraduate and 180 graduate students. We offer an ABET accredited undergraduate program, and graduate study and research for master's and doctoral degree students. Courses of study and faculty research are concentrated in the areas of: Bioengineering, Communication Theory, Computer Engineering, Computer Vision, Control Systems, Electronics, Image Processing, Opto-electronic Devices, Power, and Signal Processing. Outstanding candidates in any of the above areas will be considered. Faculty candidates should have an earned doctorate, an established research record, and be committed to an integrated program of teaching and research. Industrial experience is desirable. Priority will be given to U.S. citizens or permanent residents. Applicants should submit resumes and the names of three references to: Dr. Ronald Hoelzeman, Search Committee Chair, Department of Electrical Engineering, 348 Benedum Hall, University of Pittsburgh, Pittsburgh, PA 15261. Phone: 412-624-9676. In order to ensure full consideration, applications must be received before December 15, 1992. The University of Pittsburgh is an Affirmative Action, Equal Opportunity Employer.

Electrical Engineering Department: CTEH aff. Tel-Aviv University, Assistant/Associate Professor position, tenure track. Specialization in Communications and/or Digital Electronics. Submit curriculum vitae and references to Prof. David Moalem Maron, Director, Center for Technological Education Holon, 52 Golomb Street, Holon 58102, Israel.

The Institute for Micromanufacturing at Louisiana Tech University is inviting applications from qualified individuals for tenure track faculty, research engineers, research associates, visiting scholars, postdoctors and technician positions in the areas of optical lithography, x-ray lithography, metrology, materials science, micromechanics, and technology transfer to support the development of microelectromechanical systems (MEMS) to the prototype stage. Appointments for the faculty positions will be considered at the Assistant, Associate and Full Professor rank commensurate with qualifications, which include an earned doctorate in mechanical engineering, electrical engineering, biomedical engineering, materials science, physics, chemistry, biology or a related field, and a strong commitment to education, developing externally funded research. Group leaders, qualified at the full professor level, are being sought in several areas. The research engineer and associate positions require a minimum of a BS degree and appropriate professional experience in one of the areas mentioned above. Screening of applicants will begin immediately and applications will be accepted until the positions are filled. Some positions will not be filled until September of 1993 or later. Please send resume, names of three professional references and a brief description of teaching and research interests to Dr. Robert O. Warrington, Director, Institute for Micromanufacturing, Louisiana Tech University, P.O. Box 10348, Ruston, LA 71272-0046. Louisiana Tech University is an equal opportunity employer. Women and minorities are encouraged to apply.

Graduate Assistantships in Optics at CREOL. The Center for Research in Electro-Optics and Lasers (CREOL) at the University of Central Florida is seeking highly qualified applicants for a number of Graduate Assistantships in optics. Stipends range from $11,000 to $15,000 for 12 months. Exceptional students will be considered for assistantship enhancements up to $4,000 through the Litton Foundation and United Technologies Optical Systems. Degrees of MS and Ph.D. in Optical Sciences and Engineering, Electrical Engineering and Physics are offered at UCF. CREOL has 28 faculty positions devoted to lasers and optical sciences and engineering. The academic program includes 23 specialized courses in electro-optics and lasers as well as basic Electrical Engineering and Physics courses. Current research activities include: laser propagation, laser/material interaction, nonlinear optics, integrated-optics, infrared systems, optical signal processing, laser development, detector technology, ultrafast phenomena, x-ray sources and lithography, nonlinear optical spectroscopy, diffractive optics, thin film optics, metal vapor lasers, free electron lasers, optoelectronics, growth of nonlinear and laser host materials, superconductivity, solid state and micro lasers, and others. Applications are invited from students with an excellent academic record and fluent command of the English language. Completed applications are due by February 15, 1993. To receive an application package, write to: CREOL - University of Central Florida Graduate Affairs Committee, 12424 Research Parkway, Suite 400, Orlando, FL 32826.

Graduate Research Assistantships are available for graduate students pursuing the M.S. or Ph.D. degrees in Electric Power Systems at Clemson University. Funding is available through Clemson University Electric Power Research Associations (CUEPRA), NSF, and research contracts with power companies. Research assistantships consist of a monthly stipend and tuition fee reduction. For United States citizens, Industrial fellowships are also available. For further information, contact Dr. Adly A. Girgis, ECE Department, Clemson University, Clemson, SC 29634-0915.

Stanford University - Faculty Openings - Stanford University's Departments of Computer Science and Electrical Engineering seek applicants for a tenure track faculty position in telecommunications software. Applicants should have a Ph.D. in a relevant field, and should have a strong interest in both teaching and research. The appointment will be made at the level of Assistant Professor. Examples of sub-fields of interest include: congestion control, routing algorithms, protocol design, protocol architectures, automated network management and directory services, and software reliability within a telecommunications context. The successful candidate will be expected to teach courses, both in his/her speciality area and in related subjects, and to build and lead a team of graduate students in Ph.D. research. Stanford University is an equal opportunity/affirmative action employer and especially encourages applications from both minorities and women. Applications, including a resume, a publications list and the names of five references, should be sent by January 31, 1993 to: Professor Fouad Tobagi, Search Chairman, Department of Electrical Engineering, Stanford University, Stanford, CA 94305-4055.

Faculty Position - The Center for Microelectronics Research (CMR) at the University of South Florida invites applications/nominations for tenure-track faculty position at Assistant or Associate Professor level beginning May or August 1993. Applicants should have earned doctorate and record of outstanding industrial experience and/or university research experience in microelectronics VLSI/ULSI/WSI architecture, design, or MCM and packaging technology or test; or microelectronics materials and defects, semiconductor processing and manufacturing. Experience in the area of interconnect technology for rapid prototyping is highly desired. The successful applicant will be expected to develop a strong funded research program in his/her area of expertise. A joint faculty appointment in both CMR and the Dept. of Electrical Engineering is anticipated. CMR has benefitted from strong research funding which totals $14 million over the past four years. USF is an Affirmative Action/Equal OpportunityEmployer. Nominations/applications to Dr. Earl Claire, Director, CMR/College of Engineering, USF, 4202 E. Fowler Ave., Tampa, FL 33620, by 12/15/92.

The University of Trondheim - The Norwegian Institute of Technology - Department of Telecommunications - The Norwegian Institute of Technology is inviting applications for a position as full professor in Telecommunications. The area of specialization is Information and Coding Theory. The candidate is required to have an outstanding research record. He/she should demonstrate strong didactic skills and the ability to initiate research activities. The successful candidate will, together with the other professors in the Department of Telecommunications, be responsible for research and teaching at M.Sc. and Ph.D. levels. The Norwegian Institute of Technology has 7100 students and is part of the University of Trondheim. The Institute is collocated with the SINTEF Group, a research organization with a total of 1800 employees. Telecommunications/research is carried out in close cooperation with SINTEF-DELAB, a branch of the SINTEF Group. The total number of permanent scientific staff members within the field of Telecommunications is approximately 85. The city of Trondheim has 140,000 inhabitants. There are good public schools in the area, and also an English primary School. English is widely spoken, both at the Institute and in the community. There are excellent opportunities for outdoor activities in the vicinity, including skiing, fishing, hiking, and cycling. Further information about the position and the teaching program may be obtained by contacting Professor Nils Holte, telephone +47 7 594319, fax +47 7 592640, or Professor Tor Erik Vigran, telephone +47 7 594338. Applications close on January 4, 1993. Applications, with curriculum vitae, certificates of education and publications should be sent to the University of Trondheim, The Norwegian Institute of Technology, Personnel Section, N-7034 Trondheim, Norway.

Electrical and Computer Engineering Departments - The department of Electrical and Computer Engineering of Ecole Polytechnique is seeking candidates to fill the position of Professor - Power Systems and, depending on the availability of funds, the position of Professor - Electric Machines. The main duties of these positions include: Teaching Power Engineering every semester in both the classroom and labo-

ratory; Directing and supervising post-graduate students; Creating and executing research projects in the areas listed below; Developing and maintaining research activities in collaboration with industry. Experience in the following areas is required: Position 1: Power Systems - Application of computers for analysis and simulation: generation, transmission, distribution and utilization of electrical energy. Digital methods for solving planning, design, operation and protection problems; Flexible Alternating Current Transmission System (FACTS); Improvement of electrical energy quality (pollution and harmonic compensation); Modern computer technologies for network analysis and simulation. Position 2: Electric Machines - Motor drives of low-, medium- and high-power industrial machines for AC and DC currents; Machine-charge interaction, motor drive modeling, analog and digital control; Study and development of electrical drives including microprocessor controls, power converters and inverters; Implementation of modern methods of control (sliding system, fuzzy logic); System performance: quality of use of electrical energy, machine-converter performance, charge dynamics; Instrumentation: speed and torque sensors, power, power factor and distortion measurements. Requirements - Candidates must hold a doctorate (PhD) in Electrical Engineering or in a discipline related to the research fields described above and be members of, or eligible for membership of, the Ordre des ingenieurs du Quebec. Knowledge of spoken and written French is essential. Experience in the industry would be an asset. Starting date: January 1, 1993. Salary and conditions: Remuneration and benefits will be determined in accordance with current standards at l'Ecole Polytechnique. How to apply: Applications, accompanied by a curriculum vitae in French, photocopies of all attestations of studies, names of three references and three copies (maximum) of your most recent publications relevant to the areas mentioned above should be sent to the following address (arriving no later than November 1, 1992): Professor Bernard Lanctot, Director, Departement de genie electrique et de genie informatique, Ecole Polytechnique, C.P. 6079, Succ. A, Montreal, Quebec, H3C 3A7 Canada. In accordance with Canadian immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada. Ecole Polytechnique is an equal opportunity employer.

Iowa State University - The Department of Electrical Engineering and Computer Engineering invites applications for a tenure track position in Computer Engineering. Preference will be given to individuals with expertise in VLSI Design and emphasis on VLSI CAD, VLSI Synthesis and Circuit Simulation. The candidate will join an existing VLSI Design group in the department. Responsibilities include teaching at both graduate and undergraduate levels, conducting a vigorous research program and participating in outreach activities. Applications must possess a Ph.D. with a demonstrated potential for excellence in teaching and research. Salary and rank are commensurate with qualifications and experience. Position open date is January 2, 1993, and will remain open until filled. Applications should send a resume and the names of at least three references to: Dr. Charles T. Wright, Jr., Chairman Faculty Search, Department of Electrical Engineering and Computer Engineering, 201 Coover Hall, Iowa State University, Ames, Iowa 50011. Iowa State University is an Equal Opportunity/Affirmative Action Employer.

Faculty Positions in Computer Engineering - The Faculte des sciences appliquees of the Universite de Sherbrooke invites applications for three tenure track faculty positions in computer engineering. General Responsibilities - Teaching at undergraduate and graduate levels, specialized research in computer engineering, graduate students supervision and training, course and program management and community involvement. General Qualifications - Ph.D. in computer and/or electrical engineering; excellent communication skill, strong commitment to teaching, research and technology transfer; excellent knowledge of written and spoken French, qualifications to become member of the Ordre des ingenieurs du Quebec. Specific Qualifications - Specialization in computer engineering in order to pursue independent research in the Information, Signal and Computer (ISC) Research Group: First position: systems and networks simulation, computer architecture; meaningful experience in computer architecture and in research; Second position: microprocessor systems and computer interfaces and peripherals; significant experience in industrial automation; Third position: computer research and development in the field of numerical (microelectronics) systems and circuits; significant industrial experience. Candidates should send their resume and c.v. to: The Dean, "Concours 92-1-20", Faculte des sciences appliquees, Universite de Sherbrooke, Sherbrooke (Quebec) J1K 2R1. N.B. - Working conditions are in accordance with the collective bargaining agreement in force. The Universite de Sherbrooke is committed to the principle of employment equity and enforces ■ Job Equity Program for Women. In accordance with Canadian immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada.

University of California, Santa Cruz - The Computer Engineering Department invites applications for a faculty position at all levels (tenure-track to full professor). Contingent upon funding. Candidates are sought with research and teaching interests in imaging/image processing, as well as workstations interfaces, networking and multimedia database systems. A Ph.D. in CE, EE, CS or equivalent is required. Salary range: $46,800-$80,700. For detailed information contact: recruit@cse.ucsc.edu or recruit@ucsc-crls.bitnet, or write to: Chair, CE Faculty Search Committee, 225 Applied Sciences, University of California, Santa Cruz, CA 95064. Closing date: February 1, 1993. Please refer to #141-889 for the tenure-track level and #141-000 for the tenured level in cover letter. UCSC is an EEO/AA/IRCA employer.

Indian Institute of Technology, New Delhi: Center for Applied Research in Electronics invites applications from Indian citizens for the Bharat Electronics Chair Professor. Candidates should have a distinguished record of contributions to the theory and practice of signal processing. Please contact: Prof. P.V. Indiresan, CARE, IIT Delhi, 110016. E-mail: ind@care.iitd.ernet.in.

Government/Industry Positions Open

Electronics Engineer for NW Ohio electronic tonnage instrument & transducer manufacturing firm to design microprocessor based control instruments & peripheral subsystems; apply mathematical algorithms to integrate software/hardware using Assembly & C languages; design of signal conditioning circuits, amplifiers, remote data communication systems, interface circuits & power supplies; use SPICE to design & analyze circuit models; use Dynamic Data Exchange facility in Microsoft Excel Macros & Windows to generate statistical reports; use CAD for printed circuit boards design, schematics & systems layout. No exp. req. in above duties, but applicants will qualify with 6 mos. exp. as a software engineer using Dynamic Data Exchange facility in Microsoft Excel Macros & Windows to generate statistical reports, Assembly & C languages & CAD tools & a B.S. in Electrical Engineering with at least 1 course in each of the following fields: digital systems design, sequential machines, semiconductor devices (using SPICE), communication theory & data structures. 40 hrs/wk, M-F, 8AM-5PM, $33,500/yr. Must have proof of legal authority to work permanently in U.S. Send resume in duplicate (No Calls) to J. Davies, JO#1333812, Ohio Bureau of Employment Services, PO Box 1618, Columbus, OH 43216.

Optical Physicist/Engineer - Rome Laboratory - Hanscom Air Force Base, MA 01731. The Optical Signal Processing Group invites applications for the position of optical physicist/engineer in the areas of low-power, non-linear optical material and device physics for applications in optical signal processing technology. A PhD degree in physics or a directly related field is desirable but equivalent experience will be considered. A proven record in initiating and performing research projects involving both theory and experiments in the following technical areas is required: 1. Photorefractive materials dynamics. 2. Real-time holography and two-dimensional optical signal processing. 3. Nonlinear, as well as linear, optical signal processing technology. A publication and patent record demonstrating original contributions in these areas is required. Experience in original device design and innovative device physics is an asset. The ability to work with other scientists and engineers in a variety of areas of state-of-the-art research is essential, as is the ability to communicate effectively. Experience with devices operating at both visible and infrared wavelengths in a variety of materials is essential. Demonstrated participation in professional societies, their meetings, and symposia would be an advantage. Annual salary range: $38,861 - $50,516 (GS-12), depending on qualifications. For information and application forms, contact Sandy McKemy, 3245 ABG/DPCS, Hanscom AFB, MA 01731, (617) 377-2280. Hanscom AFB is an Equal Employment Opportunity Employer. Positions are filled without regard to race, color, religion, sex, national origin, age, marital status, handicapping condition, political affiliation or any other non-merit factor.

Senior Process Engineer - Will develop processes to enhance quality and reliability of interconnects and to reduce manufacturing complexity for advance packages and modules, characterize materials' properties and interactions, identify failure mechanisms, perform root cause analysis, and identify solutions for complex problems in the interconnects area. Must possess Ph.D. in Materials Science with B.S. in Metallurgy. Must have academic coursework/practical experience in analytical equipment, including AES, SEM, TEM, SIMS, x-ray diffraction, x-ray photoelectron spectroscopy, CSAM, and metal-ceramic, metal-metal, and metal-polymer systems required. Must have understanding of thin film materials processing and mechanical properties. Knowledge of basic statistics required. $52,440/yr. 40 hrs./wk. Qualif. applicants send resume or application letter with ad by Oct. 21st, 1992 to: AZ DES Job Service, Attn: 732A Re: 0017064, P.O. Box 6123, Phoenix, AZ 85005. Job Location: Chandler, AZ. Emp. pd. ad. Proof of authorization to work in U.S. required if hired. The Company is an equal opportunity employer and fully supports affirmative action practices.

Design Engineer for computer peripheral firm in NE Ohio. Independently design & layout computer peripheral controller & memory boards. Plan, design & appreciate engr. schematics & support documents to plan layout of boards. Use Assembly & C for programming, CADCAM tools for design and layout. Analyze designs to determine costs & compatibility with computer architecture and operating systems specifically DOS, Apple and VAX. Must have M.S. degree in Elec. or Computer Engr. w/crsework one each in Digital System Design, Control Theory, Computer Algorithm, Computer Organization & Architecture, Microprocessor Interfacing. Must know DOS, Apple, VAX, Unix operating systems & architecture, Assembly and C, Orcad, Autocad, Schema and E.E.D. for layout. Must have 18 mo. exp. of mfg. engr. or programming engr. (CNC). Exp. may be gained before, during or after degree. 40 hrs/wk, 8:00am-5:00pm, $798.37/wk. Must have legal authority to work permanently in US. Send resume & course transcript in duplicate (no calls) to J. Davies, JO#1200898, Ohio Bureau of Employment Services, PO Box 1618, Columbus, OH 43216 before 11/1/92. An Ad as result of the filing of application for permanent alien labor certification.

Research Engineer - Systems Analyst for a process control systems company located in NE

Ohio. Duties are: Conduct theoretical research to optimize new product development & engineering design for complex industrial process control systems; apply systems engineering & control theory to develop mathematical models for design of real-time electrical & electro-hydraulic control systems for specialty metals & steel mills; use the models in research aimed at investigating system design trade-offs, parameter identification, multivariable control algorithm development, computer implementation & simulation of control laws, & performance optimization; develop project schedules; prepare technical documentation and professional papers. Requires Ph.D. major in Systems Engineering or Electrical Engineering major in area of Automatic Control Systems & 1 year exp. in job duties described or in product engineering including simulation & reliability measurement, research analyzing, testing & design of new products. Must have research exp. in the areas of parameter identification & optimal control of stochastic dynamic systems theories as evidenced by two publications, either published or thesis paper, in those areas or employer testimonial. Educational background must include one graduate course each in systems identification, decision theory and applied robotics. Must have strong background in mechanical engineering as evidenced by three courses in mechanical engineering (graduate or undergraduate). Must have working knowledge of mainframe, mini, & microcomputers, preferably DEC Vax/VMS systems & related programming languages such as Fortran, Basic, & Pascal as evidenced by employer testimonials, and/or academic letters of reference. 40 hrs/wk, 8:30am-5:00pm, Mon-Fri, $45,600 per annum. Must have proof of legal authority to work indefinitely in U.S. Send resumes in duplicate (no calls) to J. Davies, JO#1200894, Ohio Bureau of Employment Services, PO Box 1618, Columbus, OH 43216.

Senior Applications Engineer - For Roanoke, VA area emp. resp. develop. new concepts of contrl. & applic. tech. in metal rolling; develop. new meth. of structuring product offerings to satisfy metal rolling applic. and effec. production of products; critical eval. tech. & bus. develop./plans to insure tech. sound & meet future needs; applic. ideas and sys. struc. to cust.; teach contrl. sys. thry.; critical eval. site perf.; problem solv. and analysis servere contrl. perf. Must have BS in elec. eng. w/8yrs. wk. exp. in automation eng. in metal rolling ind. and proj. and mgnt. leadership skills; practical site exp. commissioning & tuning adv. rolling mill automation sys.; computing skills in use of spread sheets, word proc., CAD packages, proj. mgnt. softwre. & desktop pub. sys.; demonstrated comm. skills; stocastic contrl. thry. 40hrs./wk. Hrs. 8:00-4:45, $80,000.00/yr. No OT. To apply: mail or hand carry res. w/copy of ad attached to: VEC, Dept. 3008, 1202 Franklin Rd., Rke, VA 24016-4688, JO# VA2073224 EEOE.

Drives Applications Engineer - For Roanoke, VA area emp. resp. for Canadian pulp & paper drive bus. activity support; review of customers drive sys. req. & specs.; determ. of drive sys. & contrl. equip. req.; support & prep. tech. & comm. proposals; support sales force in complex proj. and neg.; participate in tech. discussion w/customer proj. team; presentations to customer describ. functionality of proposed drive sys.; provide support to contract admin. grp. w/tech. details during eng. mfg. and commissioning stages. Must have BE in elec. eng. w/7yrs. wk. exp. in applied eng. in pulp & paper indus. Must be able to communicate and hold tech. meetings & have exp. in design & app. of drive sys. for off machine coders, supercalendars & converting equip. including co-extrusions & film lines. 40hrs./wk. 8:00-5:00, $58,100.00/yr. No OT. To apply: mail or hand carry res. w/copy of ad attached to: VEC, Dept. 3008, 1202 Franklin Rd., Rke, VA 24016-4688, JO# VA2073436 EEOE.

Electr. Engineer needed to design electrical control panels and automation systems; will use measurement methods and related problem analysis; will use analytic approach in various hardware and software applications in related field; hrs. 7:00 am - 5:30 pm $15.16/hour, $22.28/hour/overtime. Must have 4 year college degree in electr. enginrng. Must have at least 1 course in and/or experience in: turbo assembler software, microprocessor family 86 hardware, analogue 2 digital conversion techniques, data logging systems. Employer Paid Ad. Send resumes to 7310 Woodward Avenue, Room 415, Detroit, MI 48202. Reference No. 35792.

Product Development Manager to design and develop power distribution protective control systems by utilizing the application of solid state and electromechanical relaying methods for both low and medium voltage power distribution equipment; enhance existing product designs as well as develop new designs for electrical power distribution and control systems utilizing and applying engineering principles, research data and proposed product specifications meeting the latest publications by National Electrical Code, Underwriters Laboratories, American National Standards Institute and National Electrical Manufacturers Association; study proposed customer specifications and submit corresponding designs, cost analysis and value added engineering information to assist the sales representative in final negotiations; design and develop control systems for rotating electric machines at all voltage levels as well as power factor correction systems and power generation paralleling control systems; support the customers by answering all their technical inquiries as well as travel to project sites to perform all the start-up and commissioning operations. Require a Bachelor of Science degree in Electrical Engineering and six months experience as a Marketing Manager of Electrical Power Distribution and Control Systems. Bachelor's level coursework must include: a) Power Systems Analysis; b) Generalized Electric Machine Models; and c) Control Systems Design I. Experience must be in electrical power distribution and control systems design. 40 hour wk - 7am to 4pm. $37,000/yr. Send resume to 7310 Woodward Avenue, Room 415, Detroit, Michigan 48202 - Reference #58592. Employer Paid Ad.

Systems Engineer - For Roanoke, VA area emp. resp. for proposal of new hdwre. and sftwre. designs of computer based drive sys. suitable for mfg. and appl. in automation sys. eng.; proposal of func. concept, detail algorithim and implementation; specif. of hdwre. and sftwre. to be used; supp. of design by detail simulation and specify perf. req. setting forth test proc.; select develop. tools and partic. in design and test of prod. mfg. for paper and steel ind. Must have Master of Engineering or equiv. in elec. eng. w/6yrs. wrk. exp. in sys. eng. for metals ind. automation control sys. and know. of AC & DC drive charac., micro proc. control hrdwre. design, P-CAD design package, discrete control thry., real time distrib. comp. sys., distrib. sys. communication meth., simulation pack. "ACSL" and "MATHCAD"; exp. w/HP LAN analyers and HP spect. analyzers, comp. lang. "C", PASCAL, PLM and ASM, microcomputer develop. sys. and in-circuit emulators, PLM86/AMS86 compilers, linkers, locaters, ICE and I2ICE emulators, power electronics and static conversion sys. 40+hrs./wk. Hrs. 8:00-4:45; $59,000/yr. No OT. To apply: mail or hand carry res. w/copy of ad attached to: VEC, Dept. 3008, 1202 Franklin Rd., S.W., Roa., VA 24016-4688, JO# VA2080303. EEOE

Systems Engineer - For Roanoke, VA area emp. resp. provide tech. leadership on metal rolling requisitions w/customers; prep. specs. for elec. & automation equip. & func. to meet customer req.; approve eng. order on vendor material; interface w/customer to assure proper equip. design; utilize computer simulation programs to study rolling mill control problems; participate in equip. start ups at remote job sites for extended periods. Must have MS in elec. eng. w/6yrs. wk. exp. in sys. eng. for metals indus. contrl. sys. and exp. w/contrl., data handling, operator interface & perf. req. for metal rolling processes & reheat furnaces; exp. w/applic. of motors, sensors, thyristor power converters, solid state & relay sequencing, programmable controllers & computers to metal rolling processes; ability to org., sched. & lead projects; exp. in use of simulation tools & process contrl. computer applic.; programming exp. in control thry. & process modeling. 40+hrs./wk, 8:00-4:45, $64,200.00/yr. No OT. To apply: mail or hand carry res. w/copy of ad attached to: VEC, Dept. 3008, 1202 Franklin Rd., Rke, VA 24016-4688, JO# VA2073217 EEOE.

Sustaining Broadcast Engineer - For a Southeast Ohio Electronics Manufacturer - Design and test high power, high frequency and medium frequency broadcast transmitters and dummy load circuitry for technical capability in areas not currently covered by the employer's product lines. Develop technical proposals for current or future products in the high powered, high frequency broadcast transmitter line. Maintain technical currency of the employer's existing product line. Develop new or improved products for the high frequency, high powered broadcast market. Develop test specifications and/or procedures for all high power, high frequency transmission products. Provide technical expertise in ongoing proposal efforts and in the development and/or integration of purchased technologies into the employer's product lines in the high power transmission area. Direct and coordinate activities of engineers and technicians in developmental projects; coordinate design of special test equipment; resolve technical problems with production equipment; interface as required with customer and/or other technical organizations; supervise installation and commissioning of high power HP equipment at various sites as required. Requirements: B.S. in electrical engineering or academic equivalent. No experience required in the above duties, but applicants will qualify with eight years of experience in an engineering position in which the applicant worked with high power (500 kw) broadcast transmitters in high frequency band. This work must have consisted of installation and commissioning of high power broadcast systems, design, evaluation and testing of high voltage switching and distribution systems, design and evaluation of pneumatic, cooling control and servo systems as related to the high power broadcast systems. 40 hours per week - 8:00 a.m. to 4:30 p.m., Mon-Fri with some overtime. $925 per week plus $23.13 per hour overtime. Must have proof of legal authority to work indefinitely in the U.S. Send resume in duplicate (no calls) to J. Davies, JO# 1230858, Ohio Bureau of Employment Services, P.O. Box 1618, Columbus, OH 43216.

Cree Research, Inc., the world leader in silicon carbide semiconductor device technology seeks the following position: Solid-State Device Scientist with experience in analog circuit design. Will perform silicon carbide device R&D and incorporate devices into small scale demo. circuits. Advanced degree, MOS device modeling, parameter extraction and circuit simulation experience desired. Send resume to: Human Resources Department, Cree Research, Inc., 2810 Meridian Parkway, #176, Durham, NC 27713.

Operating Analysis Engineer - Job Duties: As an electrical engineer for a major elec. & natural gas utility, implement resource optimization software. Develop large scale computer programs to optimize the operation of generation & scheduling of energy purchases which consists of: analyzing present operating practices and recommending improvements, develop algorithms necessary to implement the improvements, develop software specifications test software & resolution of deviations from specifications. Develop policies & procedures on the generation operations & transactions scheduling & strategies, identify potential new transactions or modifications to existing ones. Conduct analysis & develop new contracts/modifications. Conduct detailed econ. modeling and analysis of transactions proposed by other utilities/NSP Department. Conducts long term simulations of resource plans using probablistic production costing & capacity scenario modeling. Conducts detailed econ. analysis to identify least cost resource plan. Make recommendations on capacity additions & prepares reports for regulatory agencies & mgmt. Develops avoided costs for qualifying facility non-utility generation & support the development of contracts for these. Min. Educ. Req: M.S. in Electrical Engineering - Min. Exp./Training Req: 1 yr. exp. in Electrical/Power System Engineering - Special Req: Knowledge of or exp. in power system operations with emphasis on: (a) application of optimization theory to generation & energy purchase; (b) specifications testing of large scale computer programs; (c) development & use of transaction services schedules. Programming exp. in Fortran, Pascal and C. Course work must include advanced classes in: (a) Power System Analysis

CLASSIFIED

& Design; (b) Transient Stability Analysis; (c) Power System Relaying; (d) Optimization Theory; (e) Application of Computers in Power System Operation; (f) Fault Analysis; & (g) Computational/Linear Algebra. Work outside core business hours may be req'd (e.g. evenings/ weekends.) Salary/Conditions: $3,597.00 per month. Hours: 8:00 a.m. to 5:00 p.m. Any applicant who is interested in this position may apply to the individual listed below for consideration. All applicants must be authorized for permanent employment in the United States in order to apply for the position: Send Resumes to: Ms. S. Springmeyer #2-92, MDJT-Room 203, 777 East Lake Street, Minneapolis, MN 55407.

Government/Industry Positions Wanted

Designer 1-5Ghz 1KW AM Trans. 25K 214-596-8319.

Communications Engineer: MSEE (Comm & DSP) experience in electric utility comm: fiber optics, power line carrier, and VHF radio. Computer: Turbo C, FORTRAN, QB, MSDOS, UNIX, etc. (813) 238-5996.

Universität Ulm

An der Fakultät für Ingenieurwissenschaften ist in der Abteilung Allgemeine Elektrotechnik und Mikroelektronik eine

C3-Professur

zu besetzen.

Die Forschungsschwerpunkte der Abteilung liegen auf dem Gebiet des Entwurfs hochintegrierter Schaltungen und der Integration von mikroelektronischen Systemen.

Bewerberinnen und Bewerber sollten mehrjährige Erfahrungen auf den folgenden Gebieten vorweisen können:

- Entwurf integrierter Schaltungen
- Strukturierung mikroelektronischer Systeme

Promotion sowie Habilitation oder eine äquivalente wissenschaftliche Leistung werden vorausgesetzt.

Im Rahmen des Studiums der Elektrotechnik wird von den Bewerberinnen und Bewerbern eine angemessene Beteiligung in der Lehre erwartet.

Die Universität Ulm strebt eine Erhöhung des Anteils von Frauen in Forschung und Lehre an und bittet deshalb qualifizierte Wissenschaftlerinnen nachdrücklich um ihre Bewerbung.

Bewerbungen sind baldmöglichst zu richten an den Dekan der Fakultät für Ingenieurwissenschaften, Universität Ulm, Postfach 40 66, W-7900 Ulm.

Schwerbehinderte werden bei entsprechender Eignung vorrangig eingestellt.

NATIONAL UNIVERSITY OF SINGAPORE

DEPARTMENT OF ELECTRICAL ENGINEERING

Appointments

The Department of Electrical Engineering invites applications for teaching and research appointments from candidates with a PhD degree in one of the following areas:

Computer Communications
Optical Fibre Communications
Computer Architecture and Systems
Microwave Electronics
Parallel Processing
Fault-tolerant Computing
VLSI Design
Magnetics

Besides appointments on normal 3-year contracts, visiting appointments for one to two years may be considered.

Gross annual emoluments range as follows:

Lecturer/Research Scientist	S$53,160 - 64,200
Senior Lecturer	S$58,680 - 100,310
Associate Professor	S$88,650 - 122,870

(US$1.00 = S$1.59 approximately)

The commencing salary will depend on the candidate's qualifications, experience and the level of appointment offered.

Leave and medical benefits will be provided. Depending on the type of contract offered, other benefits may include: provident fund benefits or an end-of-contract gratuity, a settling-in allowance of S$1,000 or S$2,000, subsidised housing at nominal rentals ranging from S$100 to S$216 p.m., education allowance for up to three children subject to a maximum of S$16,425 per annum per child, passage assistance and baggage allowance for the transportation of personal effects to Singapore. Staff members may undertake consultation work, subject to the approval of the University, and retain consultation fees up to a maximum of 60% of their gross annual emoluments in a calendar year.

Lee Kuan Yew Postdoctoral Fellowship

Applicants for appointment as Research Scientist may also apply for the **Lee Kuan Yew Postdoctoral Fellowship,** which will be awarded to candidates with excellent academic records and research potential and who had obtained their PhD degrees in the last few years. A stipend will be provided under the Fellowship which will be held concurrently with the candidate's appointment as a Research Scientist.

Facilities

The Electrical Engineering Department has currently an academic staff strength of 71 with 21 laboratories, all of which have excellent facilities for teaching and research. In addition, there are three externally funded research centres: Centre for Optoelectronics, Centre for IC Failure Analysis and Reliability and the Magnetics Technology Centre. Facilities include a Riber 32P Molecular Beam Epitaxy System and 2 liquid phase epitaxy systems for research into III-V compound devices. A wide range of computing resources are available, including numerous PCs, SUN Sparcstations, Microvaxes, and HP 9000 Series 300s. The University Computer Centre operates an IBM3081 KX2, and has acquired a high-speed campus-wide network directly linking the staff's PCs (now provided to every staff member) to the various computing resources, including 2 supercomputers based in the nearby Science Park. A number of large-scale research projects are in progress, including an optical LAN joint effort with Singapore Telecom and a project to develop VLSI design tools jointly with Chartered Semiconductors. The Department has spearheaded the formation of the national Institute of Microelectronics and has recently been commissioned to establish a national Centre for Wireless Communications.

Application forms and further information on terms and conditions of service may be obtained from:

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Technically speaking

What's in a (project) name?

Few tasks generate as much fervor as choosing a name for a project or product. Almost always, each new effort gets two names: one identifies it internally and the other is used for public marketing. While the public name is almost always constrained by the current marketing plan, the internal name often seems to be random or chosen on some whim.

Some project names are inspired by a current event. For instance, Texas Instruments Inc., Dallas, had products code-named Yoda and Skywalker in the early 1980s, reflecting the public interest in the *Star Wars* movies. Animals are also a popular theme, and their names are often chosen so that they somehow describe the nature of the project. A ruggedized product might be named Rhino, for example, while a new fast math coprocessor may be named Cheetah.

Then again, some names are puns that allude, directly or indirectly, to the nature of the project. Texas Microsystems Inc., Houston, Texas, used the code name Oatbran for a serial interface card it developed. There is no information as to whether it was targeted at a high-fiber environment.

Other names do not make it beyond the design table—and for obvious reasons. TI gave the name *Tsunami* to a project to develop a processor for a Sun Microsystems workstation. The Japanese word for tidal wave, it was never intended as a public name although it had interesting marketing possibilities: the word Sun surrounded by TI, and marketing slogans such as "The next wave in low-cost workstations."

Regrettably, the name would have had marketing repercussions in certain parts of the globe, most notably Japan, which attaches a strong negative connotation to this natural event. The name *Tsunami* would be as effective in Japan as a project named Big Destructive Earthquake in the United States.

Not all project names connote excitement in media promotions. Santa Clara, Calif.-based Intel Corp.'s 80x86 product family, one of the projects best known to the general population, has the curious distinction of possessing one of the most lackluster of internal product names. The trend began with the 80186, which went by the internal name P1, all the way to the 80486, internally called the P4. While the existence of the as-yet-unannounced successor to the Intel 80486DX microprocessor is not a secret, the external marketing name is still being chosen. In the interim, it is being referred to by its internal name—you guessed it, P5.

One of the more popular naming conventions is to use related names for a family of products. The animal naming convention has begotten veritable "zoos" of products at some companies. Intel in one project named a series of chips after the planets of the solar system. Such dynasties can have their drawbacks if the family name is not chosen carefully, though.

TI took a novel approach to naming its TMS320CXX family of digital signal processors (DSPs). The project manager for the TMS320C30 DSP, an ethnic Asian Indian, dubbed it Brahma, after the Indian god. A later derivative of the DSP family was named Shiva, after another Indian god. But there the naming convention stopped. One night, as the project manager was having dinner with his family, his daughter asked, "How is Brahma?" Her interest surprised him, and he realized that a project name's significance extended beyond his office.

These thoughts weighed on his mind as he searched for the name of the next member of the processor family. That one was designed to be small and powerful, but also work quickly and efficiently with other processors. The image of Santa Claus and his elves sprang to mind, and the next member of the family was named Elf. The project manager's daughter wholeheartedly approved.

Technically (mis)speaking

Technically Speaking received several letters about the measurements of breadboxes in the May issue. Several readers noted that the numbers corresponded exactly to a 9-by-9-by-12-inch box. The measurements were made in English units, to an accuracy of 1/16 inch, with a Teenage Mutant Ninja Turtle ruler borrowed from the school supply section of the department store. In keeping with *Spectrum*'s policy of encouraging the use of SI or at least metric units, the measurements were then converted into centimeters.

Some readers took issue with the accuracy of the final volume, noting that the number of significant digits carried through the calculation was incorrect. Many engineers, and in particular electrical engineers, work primarily in a single system of units and seldom encounter the problem of carrying accuracy between systems of measurement. So how does one convert accuracy between different systems of measurement?

The conversion factors for moving between English and SI units are in many cases exact, and for them an infinite precision can be assumed. One is the exact equivalence of 1 inch and 2.54 cm. Care must be taken, however, to prevent an artificial precision. For example, 2 1/16 inches converts exactly to 5.238750 cm. But this value, while correct mathematically, does not represent the correct accuracy. A bit more thought is needed.

The American National Standard Metric Practice booklet, ANSI/IEEE Std 268-1982, published by the IEEE, discusses the matter of accuracy when converting numbers between different measurement systems. "This estimate of intended precision should never be smaller than the accuracy of measurement and should usually be smaller than one tenth the tolerance if one exists. After estimating the precision of the dimension, the converted dimension should be rounded to a minimum number of significant digits such that a unit of the last place is equal to or smaller than the converted precision."

Let the breadbox measurements serve as an example. First, they all must be converted to metric without rounding. The breadbox's depth, 9 inches, converts to 22.86 cm. The accuracy of the measurement, 1/16 inch, converts to 0.15875 cm.

To determine the number of significant digits, the degree of accuracy of the measurement should be added to the converted value. An accuracy of 0.15875 cm means that the true value may vary plus or minus one-half the value, ranging from 22.780625 to 22.939375 cm. From this comparison, it is apparent that the measurement is accurate to only two places, and so the value should be reported as 23 cm. Similarly, the 12-inch measurement could vary between 30.321250 and 30.63875 cm, so the final result should be reported to no more than two significant digits.

Support is growing for the adoption of the breadbox unit. A recent article by the Associated Press concerning tests of technology destined for the U.S. Strategic Defense Initiative serves to reinforce the popularity of this orphaned unit. The article reported that "The 'kill vehicle' used in Friday's test flight, known officially as the Lightweight Exoatmospheric Projectile, or LEAP, weighs about 13 pounds and is not much bigger than a breadbox."

Incidentally, the final volume of the breadbox, incorporating the correct number of significant digits and correcting a mathematical error, should be 16 000 cm^3. The American National Standards Institute has been notified of the correction.

COORDINATOR: Kevin Self
CONSULTANT: Anne Eisenberg, Polytechnic University

PROFESSIONAL CONSULTING SERVICES

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The IEEE Press needs authors and reviewers for its series of practical telecommunications handbooks. Each handbook is designed to provide working engineers with information that links field experience with the formal standards and practices of the telecommunications industry.

The series editor is Whitham D. Reeve, a telecommunications engineer and consultant in Anchorage, Alaska. So far the series comprises two volumes: *Traffic system design handbook* and *Subscriber loop signaling and transmission handbook: analog*. Three more books are being prepared: *Subscriber loop: digital* is one, and the others are *Introduction to signaling systems and SS No. 7*, and *Power system design*.

Proposed topics for future handbooks include terrestrial radio system design, satellite earth station design, and switching and networking. The series is being developed with the IEEE Communications Society.

Prospective authors should be engineering practitioners with hands-on experience in telecommunications technology. Those interested in writing a handbook should contact Reeve at: Reeve Consulting Engineers, Box 190225, Anchorage, Alaska 99519. For information about the series and the IEEE Press, contact Dudley Kay, executive editor, at 908-562-3967; fax, 908-981-8062.

Coping with HDTV

The upcoming standardization of high-definition television (HDTV) and its impact on a broad range of technical professions will be the topic of an IEEE videoconference on Oct. 29 titled, "How will we broadcast HDTV?"

The program will cover four major topics:
- How North America will select a new standard for HDTV.
- The impact of HDTV on consumer products, multimedia, and delivery methods other than broadcast.
- How today's digital video-compression systems actually work.
- Techniques used to broadcast HDTV.

Leading the videoconference will be Jules A. Bellisio (SM), executive director, video systems and signal-processing research, Bellcore, Red Bank, N.J., who has been involved in the practical applications of digital telecommunications for over 30 years. Other presenters will be from Zenith Electronic Corp., Glenview, Ill., and the Advanced Television Systems Committee, Washington, D.C.

The broadcast will be from 12 noon to 3 p.m. EST through an interactive network (one-way video, two-way audio). The fee is US $1800 for a corporate site and $850 for a university site (per-person rates are also available).

For information, contact Judy Brady, marketing manager–videoconferences, IEEE Marketing Department, Piscataway, N.J., at 908-562-3991; fax, 908-981-8062.

The economy after the voting

An economic forecast exploring the impact on the electronics industry of the election of the next President will be featured during the IEEE's Wescon/92 conference and exhibit in Anaheim, Calif., in mid-November. Daniel H. Case III, president and chief executive officer of Hambrecht & Quist Group, and Jeanette A. Garretty, the Bank of America's head of industry analysis, will share their insights into the challenges in store for high-tech companies in southern California and throughout the United States in the post-election economy.

Wescon/92 will take place at the Anaheim Convention Center. The economic discussion will be held at the center on Wednesday, Nov. 18, 2–3:30 p.m. For information on the conference, see the Calendar listing beginning on p. 7.

Coming
in Spectrum

Software for engineers. The *IEEE Spectrum*'s annual focus report on new engineering and scientific packages for PCs and workstations returns for the third time. Innovations are a reader survey on software usage and the findings of a users' panel on the utilization of computer-aided design (CAD) frameworks. Eminent authors also assess the pros and cons of recent arrivals in the eight product categories, including:
- Logic synthesis for application-specific ICs (ASICs).
- Math and graphics visualization.
- Electromagnetic simulation and design.
- Development tools for embedded signal processing.
- Multichip module routing and placement.

Electric vehicles return. Laws requiring zero-emission vehicles on the roads are already on the books. This special report on the electric car examines the propulsion battery problem, and also discusses motor design and control, charging, and the infrastructure required.

Fuzzy logic with feedback. When their performance is unsatisfactory, adaptive fuzzy systems can change their own operating parameters, making them both more robust and more versatile. This article is the second in a series on fuzzy logic.

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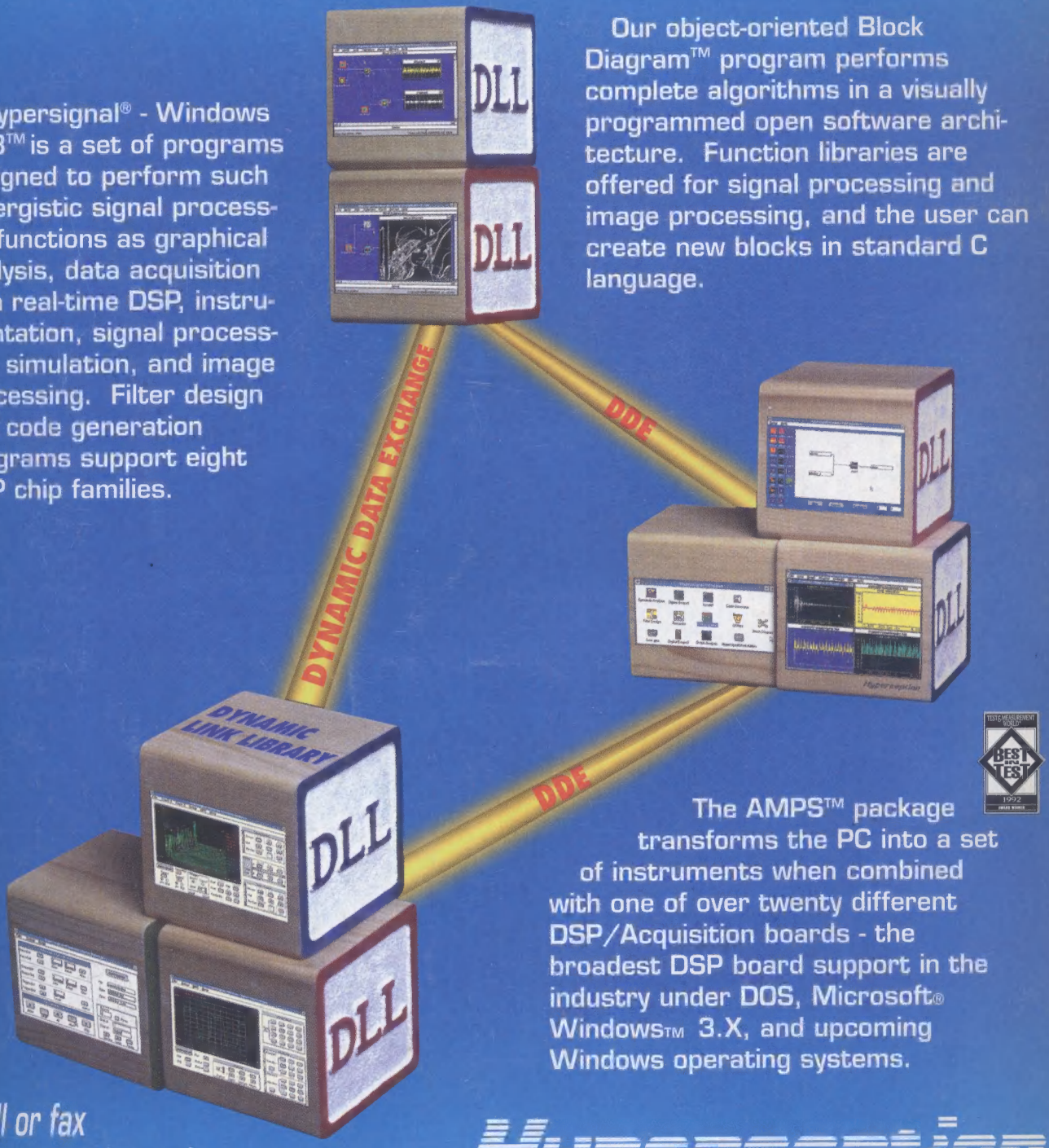

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